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INTELLIGENT DATA-ACQUISITION INSTRUMENTATION FOR SPECIAL NUCLEAR MATERIAL ASSAY DATA ANALYSIS

by
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ABSTRACT

The Detection, Surveillance, Verification, and Recovery Group of the Los Alamos Scientific Laboratory Energy Division/Nuclear Safeguards Programs is now utilizing intelligent data-acquisition instrumentation for assay data analysis of special nuclear material. The data acquisition and analysis are enabled by the incorporation of a number-crunching microprocessor sequenced by a single component microcomputer. Microcomputer firmware establishes the capability for processing the computation of several selected functions and also the ability of instrumentation self-diagnostics.

INTELLIGENT DATA-ACQUISITION INSTRUMENTATION FOR SPECIAL NUCLEAR MATERIAL ASSAY DATA ANALYSIS*

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I. INTRODUCTION

The Detection, Surveillance, Verification, and Recovery Group of the Los Alamos Scientific Laboratory Energy Division/Nuclear Safeguards Programs is presently utilizing intelligent data-acquisition instrumentation for assay data analysis of special nuclear material. The microcomputer-based instrumentation module has firmware for as many as 12 user-selected functions.

The data acquisition and analysis are enabled by the incorporation of a number-oriented (number-crunching) microprocessor sequenced by a single component microcomputer.

The microprocessor calculations are performed employing scientific notation with reverse polish notation (RPN) for data and key-level-language instruction input.

The hardware/software implementation of the microcomputer and microprocessor was performed by the Electronics Division Mini- and Microprocessor Group. The scalar hardware was designed by the Energy Division.

Microcomputer firmware establishes the capability for the user to select the display of scalar data or the computation of several selected functions. The microcomputer obtains the selected function from the input thumbwheel switch located on the module front panel. The switch also allows the user to self-test the display and to cause the microcomputer to execute instrumentation self-diagnostics.

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*Work performed under the auspices of the USDOE.

II. FUNCTIONAL DESCRIPTION

A. Neutron Data Acquisition

The neutron pulse signal from the detector is applied to the signal input BNC connector on the front panel shown in Fig. 1. Measurement is controlled by three push-button switches. The START push button initiates a measurement cycle. The measurement cycle is terminated by the variable N, the total number of time bins used, reaching a design parameter number of approximately one million, or the activation of the STOP button by the operator. Any termination results in a calculation and display on the light emitting diode (LED) display of the selected function data. The RESET push button reinitializes counting control prior to beginning or repeating a measurement cycle with the START push button.

The TIME/CHANNEL selector switch provides operator selection of the duration T of the desired count time interval, which is determined by the detector dieaway time. The dead time τ is set by a three-digit thumbwheel switch.

For each time bin N_i, the neutron count C_i is accumulated and added to $\sum C_k$. The neutron count accumulated for each time bin N_i is also squared and added to $\sum C_k^2$. Each of the three variables $N = \sum N_i$, $C = \sum C_k$ and $C^2 = \sum C_k^2$ is accumulated in an 8-digit binary coded decimal (BCD) counter string. Therefore, each variable is represented by a 32-bit value.

A block diagram of the electronics is shown in Fig. 2. When a measurement cycle is completed, a data-ready signal is generated by the hardwired logic circuitry of the counting control. These data are then processed by the scientific calculating system. A hexadecimal thumbwheel switch, FUNCTION SELECT, commands data input display of N, C, and C^2 for positions 13, 14, and 15, respectively. Position 0 commands the diagnostic routine. Positions 1 through 9 command computation and display of one of the 9 algorithm equations possible for implementation.

B. Scientific Calculating Capability

The scientific calculating capability is established with a number-oriented microprocessor sequenced by a single component microcomputer. A MOS/LSI number-oriented microprocessor provides the scientific calculating

capability with RPN data format. Input data sequencing, computation processing, and display of the results are controlled by a single component microcomputer.

The 64 preprogrammed functions of the National Semiconductor MM 57109 MOS/LSI number-oriented microprocessor* include the following:

Arithmetic - plus, minus, multiply, divide, add to memory, subtract from memory, multiply memory, divide memory, reciprocal;

Trigonometric - sin x, arc sin x, cos x, arc cos x, tan x, arc tan x, degrees to radians, radians to degrees;

Logarithmic - log x, ln x, e^x, 10^x;

Others - x, x^2, y^x, .

The microprocessor contains five internal 12-digit registers, X, Y, Z, T, and M, that are available to the user. Operational controls include number entry, decimal point, change sign, enter, halt, roll stack, pop stack, exchange X and Y, exchange X and M, store X to M, recall M to X, shift left or right mantissa digits, and master clear.

Six-bit instructions (key level language) and BCD data are sequenced into the microprocessor through 74LS174 latches. A hold line synchronizes the execution. Character-serial BCD outputs, digit address strobe, and ready signal are monitored through a tristate octal buffer 81LS95.

The microprocessor requires +5 V and -4 V power supplies. The microprocessor also requires a 400-kHz oscillator to obtain typical computation execution times. A CMOS 4069 hex inverter package (also supplied to +5 V and -4 V) and an RC network provide the oscillator input. All other devices operate from the +5 V supply. Representative typical execution times for an add function and a sin function are 22 ms and 562 ms, respectively.

The single component microcomputer sequencing the microprocessor is the Intel 8748 8-bit Single Component Microprocessor. The microcomputer is a totally self-sufficient 8-bit chip using Intel's N-channel silicon gate MOS

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*Reference to a company or product name here or elsewhere in this report does not imply approval or recommendation of the product by the University of California or the US Department of Energy to the exclusion of others that may be suitable.

process. The microcomputer contains a 1-K words by 8-bit byte EPROM program memory, a 64-words by 8-bit byte RAM data memory, 27 input/output (I/O) lines, and an 8-bit timer/counter in addition to the on-board oscillator and clock circuitry. The 8,192-bit EPROM can be cleared by an ultraviolet light and then electrically programmed. The EPROM program memory storage provides the system with the capability of a fully programmable calculator with program retention when the system is turned off.

The microcomputer is designed to be an efficient controller, as well as an arithmetic processor. The 96 instructions of the instruction set have extensive bit handling capability, as well as facilities for both binary and BCD arithmetic. These instructions include decimal adjust, swap upper 4 bits with lower 4 bits of accumulator, and exchange lower 4 bits of accumulator with those of a data memory register.

The I/O variables are stored in the microcomputer data memory as detailed in Fig. 3. Each variable is specified by an 8-digit mantissa, 2-digit exponent, and a sign bit for the mantissa and exponent. The 16-digit display uses a digit for each sign, two digits to repeat the commanded function select corresponding to the display value, one blank digit to separate the function select and mantissa digits, and one blank digit to separate the mantissa and exponent digits.

III. HARDWARE DESCRIPTION

The single component microcomputer monitors the START and RESET push buttons and the hardwire logic signal, data ready. These signals, as well as the three input variables and front panel data, are input to the microcomputer through Intel 8243 I/O expanders. The expander is an I/O device designed specifically to provide I/O expansion of the single chip microcomputer. The device is fabricated in 5-V NMOS, operates from a single supply voltage, and supplies high current capability.

The 8243 consists of four 4-bit bidirectional static I/O ports and one 4-bit port that serves as an interface to the microcomputer. The 4-bit multiplexed instruction and data bus allow multiples of the 8243 to be added to the same bus. The I/O ports of the 8243 serve as a direct expansion of the resident I/O facilities of the microcomputer that are accessed by their own MOV, ANL, and ORL instructions.

The variable input multiplexing circuitry was minimized by using 16-line to 1-line multiplexers (two per variable). Therefore, an input from ports P7 and P6 reads two bits of each variable as selected by port P5. The microcomputer software program executes a series of MUX control outputs and port inputs to read and recombine the three variables in data memory for computation processing.

The 16-digit LED display is controlled by the Intel 8279 programmable keyboard/display interface device. The 8279 is a general purpose programmable keyboard and display I/O interface device. The 8279 display portion provides a scanned interface for LED, incandescent, and other display components. The 8279 contains a 16 by 8 RAM that can be organized into dual 16-characters by 4-bit arrays. The RAM can be loaded or interrogated by the microcomputer.

Both right entry, calculator, and left entry typewriter display formats are possible. Both read and write of the display RAM can be done with autoincrement of the display RAM address. For this application, the 16 x 8 RAM stores the decimal point command and the microcomputer generated 7-segment code for each digit.

A quad CMOS RS latch 4044 is used to store front panel push-button data for interrupt generation and/or I/O polling by the microcomputer during program execution and diagnostic checking.

The data format for input parameters, constants, and computation results in scientific notation with an 8-digit mantissa and a 2-digit exponent. Figure 3 details the six bytes used to store the data format in the RAM. A 4-bit nibble is used to store the decimal point location (if floating point notation is desired). A second 4-bit nibble defines the mantissa sign, exponent sign, and 1 bit to indicate that the data are in the process of being updated or loaded (complete 6-byte transfer has not yet been accomplished). This allocation is determined primarily by the microprocessor output free-running 4-bit BCD character-serial transfer.

IV. SOFTWARE DESCRIPTION

The main operational program flowchart is shown in Fig. 4. The power on reset on the external RESET initializes the applicable microcomputer software registers and clears flag ϕ ($F\phi = \phi$). The function select thumbwheel switch is

debounced with a software routine that requires equality of three consecutive switch inputs, 10 ms apart. The input switch setting is used as the function code FC. Minimal display testing is accomplished if the function code is (0 or 10, 11, 12).

If data has not been acquired, the program waits for the START push button. The interrupt routine (Fig. 5) loads a register with data indicating which push button initiated the interrupt. This register is tested whenever the appropriate switch action is required to continue main program execution.

Each display digit indicates a "dash" until the START is obtained. Then the microcomputer provides a real-time software display of elapsed time until data are acquired.

Then the function code is again examined to display the data (FC = 13, 14, or 15). Otherwise the equations are calculated per the flowchart in Fig. 6. Each equation is processed per the flowchart shown in Fig. 7.

The incorporation of the number-oriented microprocessor or calculator chip or number-cruncher unit established a unique system design feature in the area of task generation. Similarity of the microprocessor operation to hand-held calculators, such as the Hewlett-Packard HP-21 or the National Semiconductor NOVUS 4520, the Scientist, allows the system designer to develop task modeling on readily available hand-held calculators. This feature eliminates the need for the system designer to become familiar with the internal operation, the instruction sets, and/or the assembly languages of the microprocessor and microcontroller. Parameter variations and accuracy studies can therefore be accomplished prior to final task coding.

Part of page 3 of the program memory is allocated to the key-level-language store. This memory assignment prevents significant main program software changes if the calculation sequence is changed or updated.

The front panel function selection position (1 through 9) is summed with the base address of a table that points to the starting address of the specific key-level language.

The SYNC routine provides the handshaking synchronization between the microcomputer HOLD signal and microprocessor READY signal. This initialization prepares the microprocessor for data/instruction entry.

The KEYCMD ACTION software uses the pointer to an address on the memory page containing the key-level language to read the next key command action. A key command action can be one of four types as shown in Fig. 7. The key command is examined and processed according to the flowchart until a program end is detected. Then the result is loaded in the 8279 display RAM that controls the LED display.

If the key command is an instruction (multiply, for example), the 6-bit code for multiply is entered into the microprocessor by the KEY IN subroutine.

If the key command is a variable, the VARSEQ variable sequence subroutine calls the KEY IN subroutine sequentially for each digit until the variable is entered. The VARSEQ subroutine processes a variable stored in RAM by requiring only the RAM starting address.

If the key command is output, the RDSEQ read-sequence subroutine reads and stores the microprocessor output, which is also in bit-parallel digit-serial form. The output is free running, and therefore, the microcomputer must be fast enough to read and store each byte before the next output byte is presented.

A. Software Design Procedure

The microcomputer program memory was written in ASM-48 Assembly Language, which is the highest level language available for the 8748. The assembler features macro capability as well as conditional assembly options.

The software source program was entered onto a double-density floppy disk. The microcomputer development hardware consisted of the Intel Series II Intellec Microcomputer Development System. This system includes an integral CRT display, an integral keyboard, a dual double-density floppy disk, a line printer, and an ICE-48 in-circuit-emulator package. The hex object code was downloaded to a PROMPT-48 for programming the microcomputer EPROM. The ICE-48 was used to initially debug the software and finally the unit hardware prior to EPROM programming and installation.

B. Self-Test Diagnostics

A self-test diagnostic routine was written to initially test all front panel functions and the run ability of the microcomputer. Each front panel switch is read and displayed in the 16-digit display. This testing allows the operator to test the front panel components operation and interconnecting

wiring both during initial checkout and upon failure repair. The diagnostic routine and operational program exceeded the 1-K program memory space. Therefore the diagnostic routine was placed in a diagnostic microcomputer that is swapped with the main program microcomputer during testing.

V. SUMMARY

The Detection, Surveillance, Verification, and Recovery Group of the Los Alamos Scientific Laboratory Energy Division/Nuclear Safeguards Programs is now utilizing intelligent data-acquisition instrumentation for assay data analysis of special nuclear material. The data acquisition and analysis are enabled by the incorporation of a number-crunching microprocessor sequenced by a single component microcomputer. Microcomputer firmware establishes the capability for processing the computation of several selected functions and also the ability of instrumentation self-diagnostics.

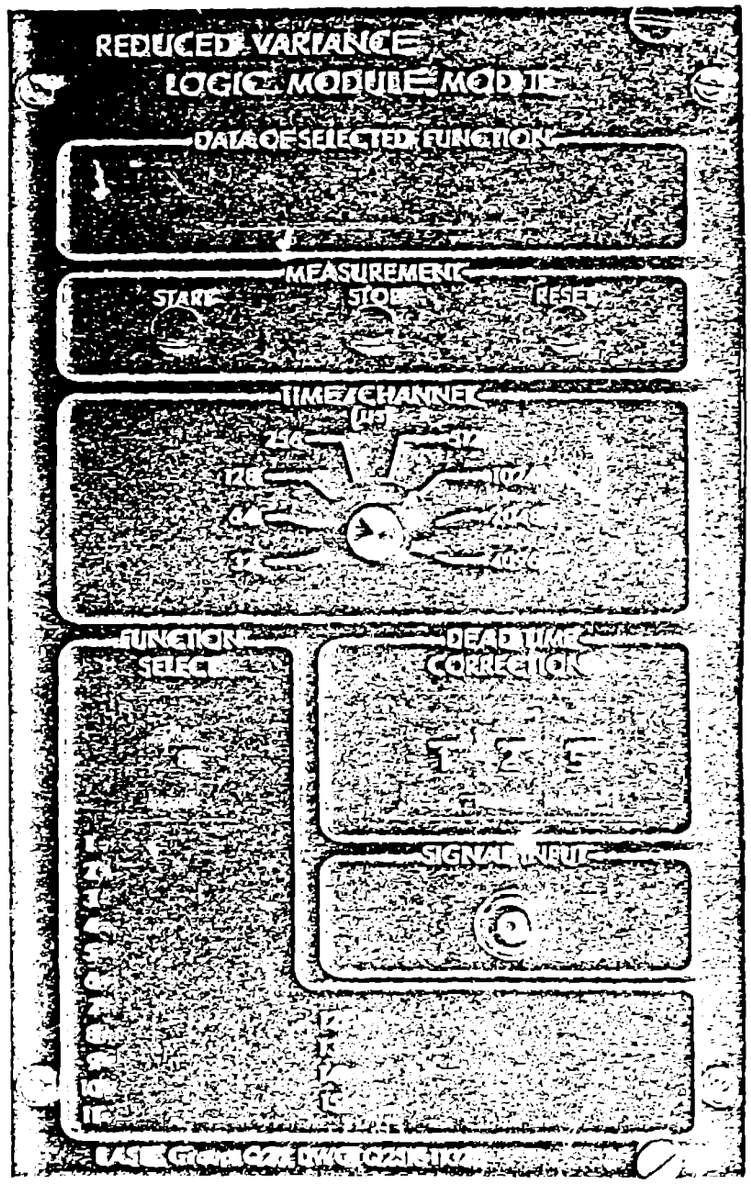

FIGURE 1. MODULE FRONT PANEL

FIGURE 2. BLOCK DIAGRAM

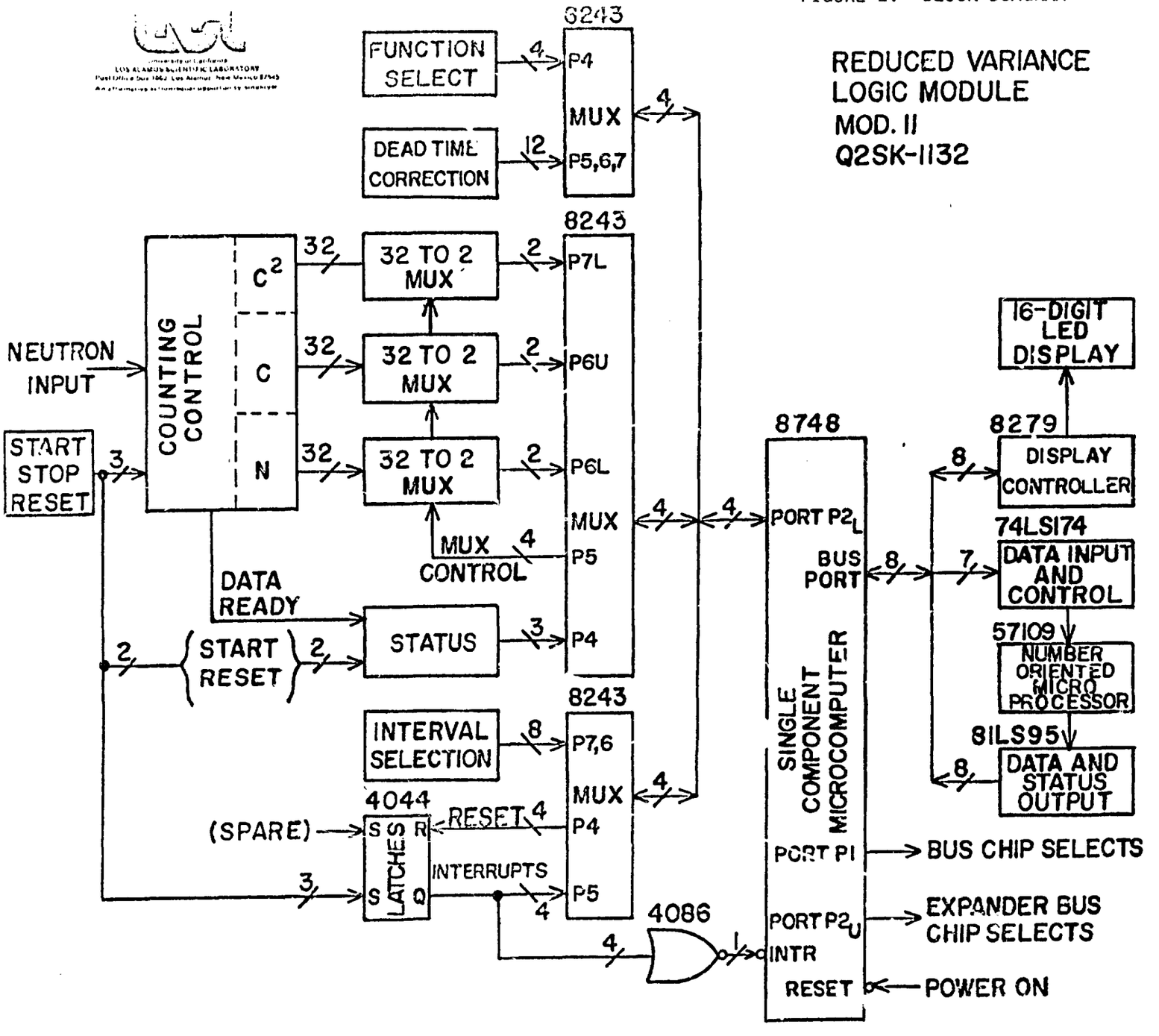

FIGURE 3
6-BYTE RAM ALLOCATION FOR VARIABLES

BIT NO / ADDRESS	7	6	5	4	3	2	1	0
BASE+5	E2				E1			
BASE+4	U	.	ES	MS	M8 (MSD)			
BASE+3	DP				M7			
BASE+2	M6				M5			
BASE+1	M4				M3			
BASE	M2				M1 (LSD)			

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FIGURE 4
MAIN PROGRAM FLOWCHART

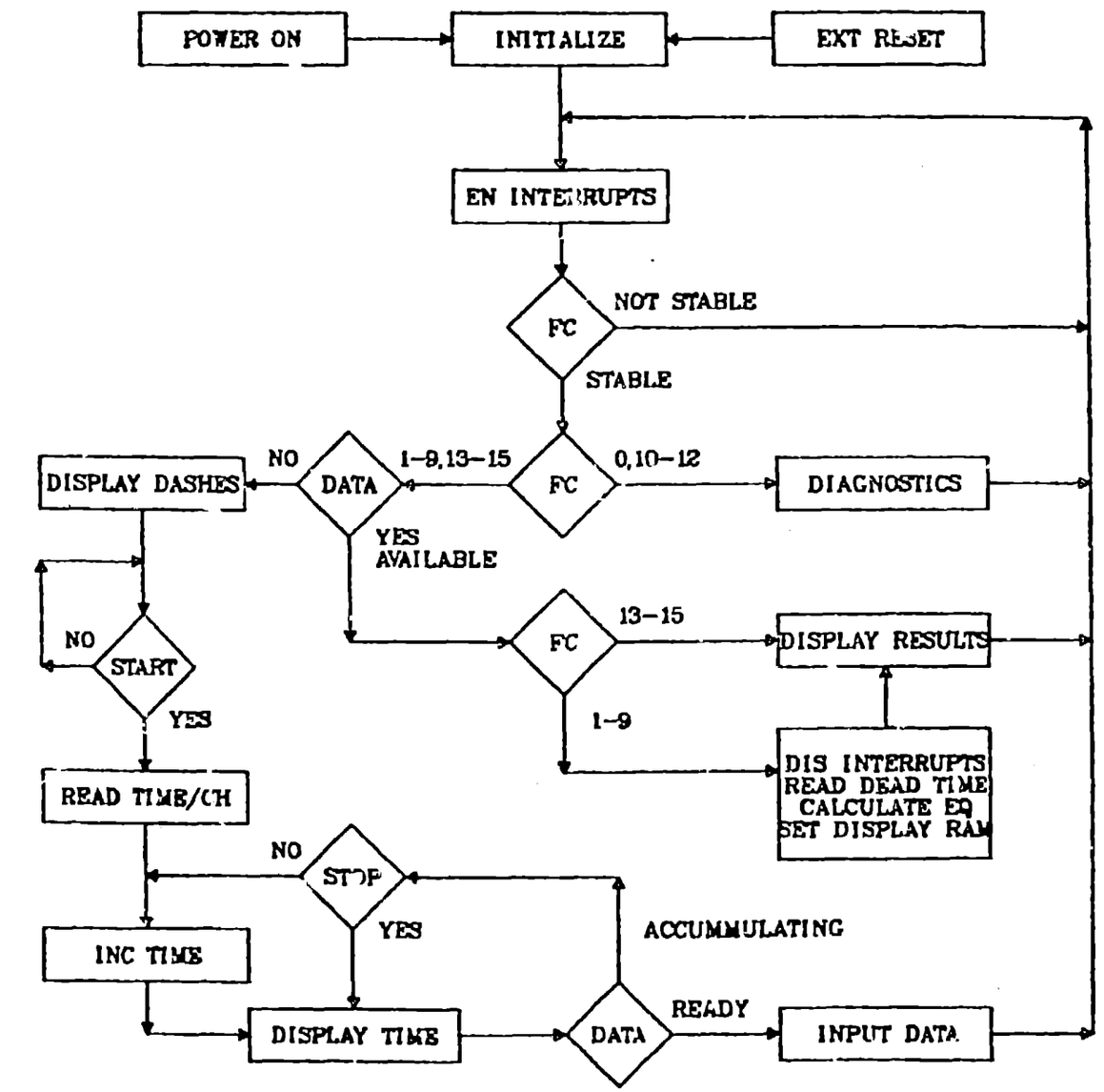

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FIGURE 5
EXTERNAL INTERRUPT FLOWCHART

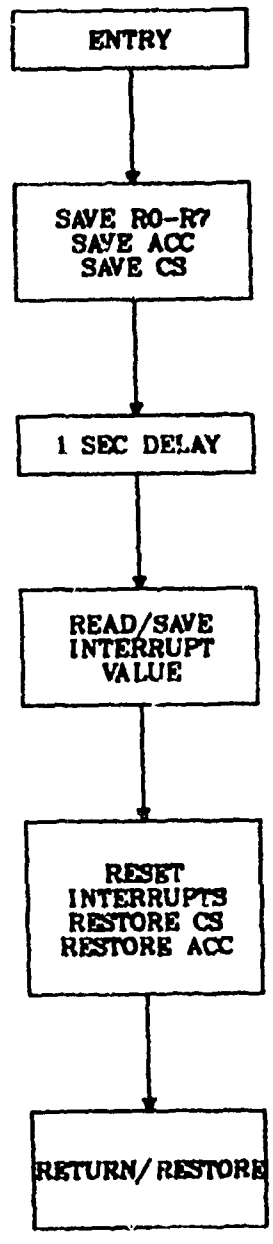

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FIGURE 6
REDUCED VARIANCE CALCULATION EQUATION-SEQUENCE FLOWCHART

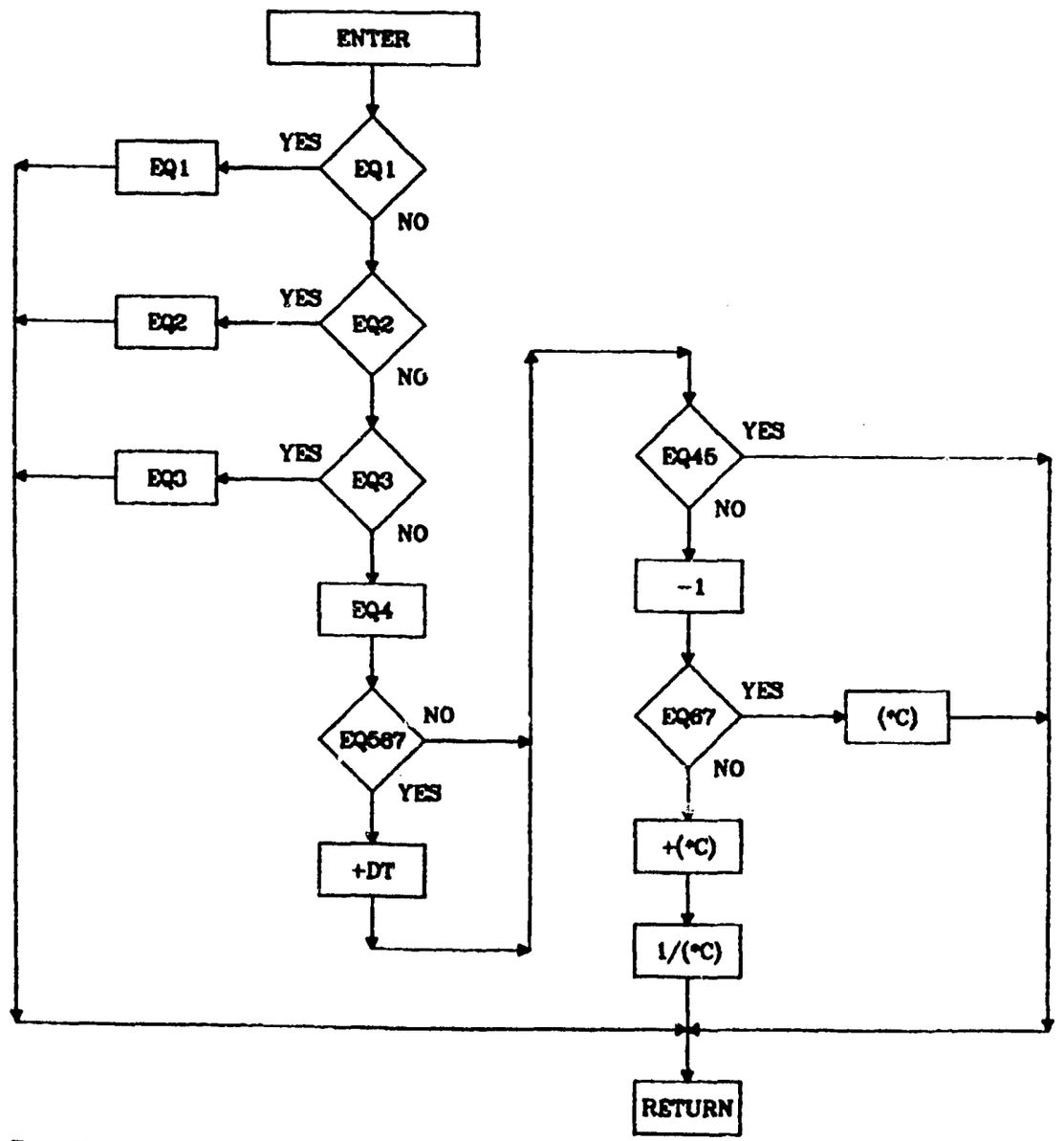

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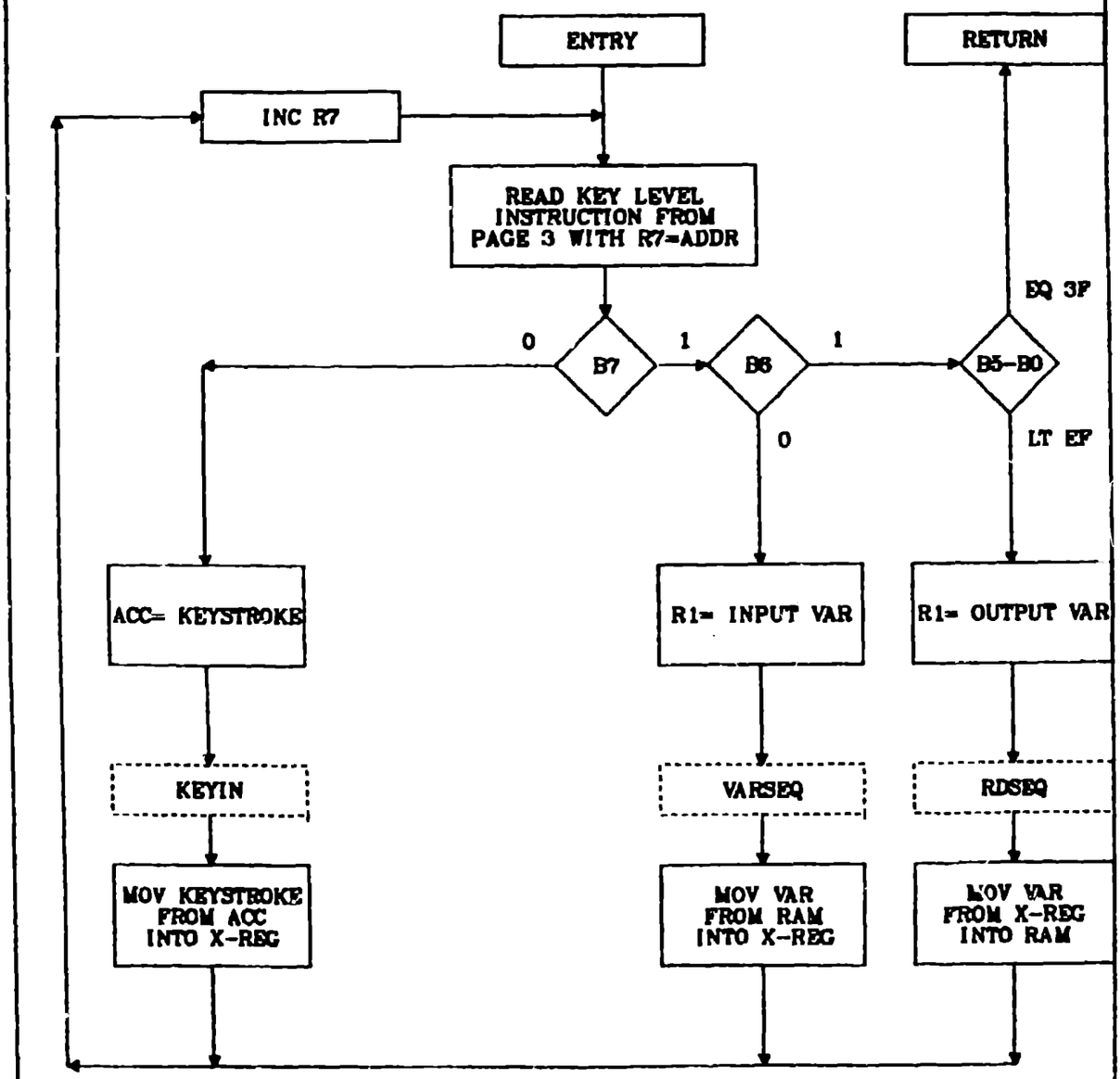
FIGURE 7
REDUCED VARIANCE/FEYNMAN VARIANCE CALCULATION SEQUENCE FLOW CHART



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