Proceedings from the Conference on –

High Speed Computing

The Art of High Speed Computing April 20–23, 1998







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Compiled by Kathleen P. Hirons Manuel Vigil Ralph Carlson



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Monday, April 20, 1998

Keynote Session:

Keynote Address: Billions and Billions Steve Wallach, CenterPoint Venture Partners

Tuesday, April 21, 1998

Session 1: The Stockpile Stewardship and Management Program

Stockpile Stewardship and Management Program Larry Ferderber, LLNL

Predictability, and the Challenge of Certifying a Stockpile Without Nuclear Testing *Ray Juzaitis, LANL*

Session 2: The Challenge of 100 TeraFLOP Computing

100 TeraFLOPs and Beyond, an Industry View into the Future Panel Discussion: Moderator—John Morrison, LANL and Mark Seager, LLNL; Panelists—Tilak Agerwala, IBM; Greg Astfalk, Hewlett-Packard; Erik Hagersten, Sun Microsystems; Richard Kaufmann, Digital Equipment Corp.; Steve Oberlin, SGI/Cray.

Session 3: ASCI Alliance

ASCI Alliances Program Ann Hayes, LANL

Session 3.5: Hardware Design

The Next Fifty Years of Computer Architecture *Burton Smith, Tera Computer Company*

Banquet

Adversarial Inspection in Iraq: 1991 and Thereafter Jay Davis, LLNL

Wednesday, April 22, 1998

Session 5: Student Session

Full Wave Modeling of Signal and Power Interconnects for High Speed Digital Circuits *Gary Haussmann, University of Colorado*

Simulating the Physical-Biological Factors Affecting Abundance of Calanus finmarchicus in the Gulf of Maine *Wendy Gentleman, Dartmouth College*

Session 6: News You Can Use

The Next Generation Internet *Bob Aiken, DOE*

Petaflops Computing: Opportunities and Challenges *David Bailey, LBNL*

President's Information Technology Advisory Committee (PITAC): A Mid-Term Report *David M. Cooper, LLNL*

Thursday, April 23, 1998

Session 7: Chip Technology for Large Scale Systems

Processing-in-Memory: Past and Present *Ken Iobst, IDA/CCS*

High Volume Technology for HPC Systems *Justin Rattner, Intel*

Session 8: Reality Check

High Performance Computing and the NCAR Procurement—Before, During, and After *Bill Buzbee, NCAR; Jim Hack and Steve Hammond, National Center for Atmospheric Research*

Economies of Scale: HPC in the Next Millennium *Gary Smaby, Smaby Group*

Session 9: Future

The Other Side of Computing *William Trimmer, Belle Mead Research, Inc.*

Crystalline Computation Norm Margolus, MIT

Quantum Computing Emanuel Knill, LANL

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Abstract

This document provides a written compilation of the presentations and viewgraphs from the 1998 Conference on High Speed Computing. "The Art of High Speed Computing," held at Gleneden Beach, Oregon, on April 20 through 23, 1998.



BILLIONS & BILLIONS

STEVE WALLACH CENTER POINT VENTURES WALLACH@CENTERPOINTVP.COM

ASPECTS OF BILLIONS

- Raised to the power (giga, tera, peta, exa)
- The inverse (nano, pico, femto, atto)
- In the computer industry they are closely related. From a technology and investment perspective
- US government policy must be consistent with industry trends. (the ultimate venture capitalist)





PRESENTATION OUTLINE

- Fundamental Laws- Physics
- Trends in Telecommunications
- Trends in Semi-conductors
- Trends in Computer Architecture
- Draw some conclusions
- US Government Policy

FUNDAMENTAL LAWS



- C Speed of light
- Power Consumption
- Propagation Delay





POWER CONSUMPTION

 $\overline{P \cup C^* V^2^*} F$

- C= capacitance
- V= voltage
- F= frequency

PROPAGATION DELAY

- Lossless Line Time $= \sqrt{LC}$
- Lossly Line

Time = $L^* \sqrt{\varepsilon_r / c_o}$ ε_r = Dielectric Constant c_o = Speed of Light





OTHER CONSTRAINTS

- Cost of Investment I (billions)
- Size of Market M (millions)
- L'Hospital's Rule of Profit
 - Profit = dM/dI
 - as I approaches infinity
 - as M approaches K (sometimes 0)
 - result is { 1 (success) | 0 (failure)}
- The government uses different rules



- Advances in *PHOTONIC* (mainly *WDM*) technology.
- TERAHZ (THz) requirements
- All optical networks (AON)
- Effect on digital computer architecture
- The next supercomputer topology
 - www.ll.mit.edu/aon/
 - Lemott, et. al., " low-cost WDM", Aug. 97, IEEE summer topicals, Montreal.







WDM ARCHITECTURE















SEMI-CONDUCTORS

- Lets examine what is driving the *I* (investment) in our equation for success.
 - Information from 1997 SIA report (www.semichips.org)

THE COST OF "FABS"



- 2 billion and climbing
- One per continent?
- Put on the moon?
- Only million piece design can be made?







UNDERLYING REASONS



- 300 mm (12inch) wafers
- Billions to replace 8 inch fabs.
- Good news: keeps costs of chips down







HOW WE GET THERE

Technology Generation	250 nm	180 nm	150 mm	130 nm	100 nm	70 nm	50 mm
Numerical Methods							
Linear solvers—equations/minute	100k	150k	250k	250k	2.5M	5M	5M
Parallel speedup	_	4	6	9	16×	30×	50×
Grid reliability (ppb)	300	180	120	90	26	14	7
MFLOPS* required	50	80	400	1000	4000	8000	8000
MC noise	NA	NA	NA	0.05	0.02	0.01	0.001
Simulation Environments							
l'ime needed for statistical sim.	10 weeks	6 weeks	4 weeks	2 weeks	2 weeks	1 week	1 week
Time needed for multi-tool initial problem setup	4 weeks	2 weeks	Jweek *	4 days	2 days	2 days	2 days
Correct data analyses per mprovement cycle	0.1	1	1	1	2	4	10
olutions Exist	Solutions Be	ing Parsue	1	X	No Known	Solution	

HOW WE GET THERE







WHAT WE GET

Table 3	Perforn	nance of .	Package	d Chips	_	
YEAR OF FIRST PRODUCT SHIPMENT	1997	1999	2001	2003	2006	2009
Technology Generations Dense Lines (DRAM Half-Pitch) (nm)	250	180	150	130	100	70
Isolated Lines (MPU Gates) (nm)	200	140	120	100	70	50
Number of Chip I/Os						
Chip-to-package (pads) high-performance	1450	2000	2400	3000	4000	5400
Chip-to-package (pads) cost-performance	800	975	1195	1460	1970	2655
Number of Package Pins/Balls	200	5- 5-	b.	5	5	
ASIC (high-performance)	1100	1500	1800	2200	3000	4100
MPU/controller, cost-performance	600	810	900	1100	1500	2000
Cost-performance package cost (cents/pin)	1.40-2.80	1.25-2.50	1.15-2.30	1.05-2.05	0.90-1.75	0.75-1.50
Chip Frequency (MHz)						
On-chip local clock, high-performance	750	1250	1500	2100	3500	6000
On-chip, across-chip clock, high-performance	750	1200	1400	1600	2000	2500
On-chip, across-chip clock, cost-performance	400	600	700	800	1100	1400
On-chip, across-chip clock, high-performance ASIC	300	500	600	700	900	1200
Chip-to-board (off-chip) speed, high-performance (Reduced-width, multiplexed bus)	750	1200	1400	1600	2000	2500

WHAT WE GET

Table 24 Product Critical Level Lithography Requirements

Year of First Product Shipment Technology Generation	1997 250 nm	1999 180 nm	2001 150 nm	2003 130 nm	2006 100 nm	2009 70 nm	2012 50 nm
Product Application							
DRAM (bits)	256M	1G	_	4G	16G	64G	256G
MPU (logic transistors/cm ²)	4M	6M	10M	18M	39M	84M	180M
ASIC (usable transistors/cm ²)*	8M	14M	16M	24M	40M	64M	100M
Minimum Feature Size (nm)**							
Isolated lines (MPU Gates)	200	140	120	100	70	50	35
Dense lines (DRAM Half Pitch)	250	180	150	130	100	70	50
Contacts	280	200	170	140	110	80	60
Development capability (minimum feature size, nm)	140	120	100	70	50	35	25
Gate CD control (nm, 3 sigma at post-etch)**	20	14	12	10	7	5	4
Product overlay (nm, mean + 3 sigma)**	85	65	55	45	35	25	20





HOW WE USE IT

• TRENDS IN COMPUTER ARCHITECTURE



GENERAL VIEWS 2 TO 4 YEARS 10 YEARS (USING SIA STUDY)







DIGITAL SIGNAL PROCESSOR









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J	AVA Vs C+-	+
FEATURE	JAVA	C++
Memory Management	Garbage collected	Explicit Memory Freeing
Multi-threading	YES (Mesa-style)	NO
Inheritance Model	Simpler (separate sub- typing)	Complex
Exception handling	Supported	Sporadic
Parametric type	Does Not	Has template
Type casts	Checked Thus easier to write protected subsystems	Unchecked (pointer ←→ integer)
		26





SO WHAT HAPPENS?

- Fundamentally the following architecture evolves:
 - PIM (processor in memory) or System-on-a-chip
 - more memory bandwidth
 - lower latency
 - consistent with PC pricing and technology curves







INTERCONNECT TYPE

• SOFTWARE

- Message Passing
- Distributed Shared Memory (DSM)
- Cache Only (COMA)
- Object oriented
- Emulated DSM (e.g.. Threadmarks)

INTERCONNECT TYPE

• HARDWARE

- Hierarchical number of levels is a function of the number of cpu's.
- Physical combination of copper and photonic. Ultimately *WDM* will play an important role in external chip interconnects.





NEXT ARCHITECTURES

- Short Term 2 To 4 years- low performance - System-on-a-chip (SOAC)
- Long Term 10 years (using SIA study)
 - High Performance
 - Supercomputing
- US Gov't R&D Policy













ARCH. - LONG TERM - 2009 DESIGN ASSUMPTIONS

- 9 million transistors vliw/risc core with first level cache.
- 2nd. Level cache rule of thumb. 1/4 to 1/2 mbyte per 100 mflops peak.
- 96 mbyte 2nd. Level (6 Inst, 90 data)
- 170 watts
- .6 to .9 volts power supply















US GOVERNMENT POLICY

- Examine the Past
- Use Tops 500 LINPACK
- Observe Venture Capital Investments
- What should happen in the future

























VENTURE CAPITAL PROFILE







US GOVERNMENT POLICY

- Provide seed money high risk/reward (darpa, nsf, dod, doe)
- Further national defense initiatives
- Begin the trickle down, technology xfer. What starts out as a US Gov't special becomes COTS after 1 or 2 generations
- Keep the US the most advanced and competitive in the world
- www.hpcc.gov/talks/petaflops-24june97







Stockpile Stewardship Program (U)

1998 Conference on High Speed Computing Gleneden Beach, Oregon April 20-23, 1998



Lawrence J. Ferderber Deputy Associate Director for National Security Lawrence Livermore National Laboratory

Lawrence Livermore National Laboratory, P.O. Box 808, Livermore, CA 94551

NS-98-031.1

The President tasked DOE to help maintain the nuclear deterrent through the Stockpile Stewardship Program

"... I consider the maintenance of a safe and reliable nuclear stockpile to be a supreme national interest of the United States."

"I am assured by the Secretary of Energy and the Directors or our nuclear weapons labs that we can meet the challenge of maintaining our nuclear deterrent under a Comprehensive Test Ban Treaty through a Science-Based Stockpile Stewardship program without nuclear testing..."

"In order for this program to succeed, both the Administration and the Congress must provide sustained bipartisan support for the stockpile stewardship program over the next decade and beyond. I am committed to working with the Congress to ensure this support."

"As part of this arrangement, I am today directing the establishment of a new annual reporting and certification requirement that will ensure that our nuclear weapons remain safe and reliable under a comprehensive test ban."

- August 11, 1995







Today the stockpile is safe and reliable, but we already require a Stockpile Stewardship Program to keep it that way

- Today's stockpile has a good "pedigree" based on
 - Nuclear tests
 - An experienced workforce
 - State of the art design (then)
- But
 - The stockpile is aging beyond our experience
 - Refurbished components will be made by new processes, in new plants by new people
 - Our experienced workforce is retiring
 - We have no nuclear tests to verify the validity of our decisions
- We need a program that will:
 - Attract and train a new workforce
 - Be able to assess the effect of changes in the stockpile
 - Certify that refurbished components are functionally equivalent to the original ones

NS-98-031. 3

Like every other technological object, a nuclear weapon ages and sometimes we are surprised when we test it



- One-point safety
- Performance at cold temperatures
- Performance under aged conditions
- Marginal performance
- Degradation of various key materials
- Pit quality control

- Metal components cracking
- Yield-select problems
- HE degrading
- HE cracking
- Detonators corroding
- Detonator system redesign
- Metal components corroding





The Stockpile Stewardship Program responds to the the store to the store the

- We have experimental data from nuclear tests which indicate that details matter – remanufactured components sometimes behave anonymously
- Current experimental and computational capabilities are not sufficient to preclude that these anomalies will occur in the future
- Without nuclear testing, we must take the conservative approach in proving our fixes are real fixes which do not introduce new problems
- We must also develop a strategy to deal with the "unknown anomalies" (e.g. Challenger O-ring) ... including residual design flaws that have not yet manifested themselves
- The stockpile will continue to age and we will be required to deal with changes to almost every components

The SSP approach is not without risk

NS-98-031. 5



Replicating nuclear weapons would be more difficult (impossible) than replicating rocket motors





The SSP provides integrated capabilities to address DoD's near-term and longer-term issues

Four SSP Strategies

- Surveillance
 - to monitor, maintain and predict the condition of the stockpile
- Assessment & Certification
 - of the consequences of change
 - that modifications and maintenance do not degrade warhead safety and reliability
- Refurbishment
 - design and manufacture of refurbished components
- Tritium replacement



NS-98-031. 7

Our surveillance program is being expanded to meet the needs of an aging stockpile

- How do weapons age?
- What are the most likely issues?
- How will these issues affect performance and safety?
- When do components need to be refurbished?



Assessment of disassembled components



Interstitial helium



Forensic surveillance techniques





The new complex must refurbish/replace components counter age, performance, or safety degradation



Plutonium pits Los Alamos, New Mexico



Assembly expertise

These new plants, people and processes must be certified to be functionally equivalent those originally used

NS-98-031. 9











NS-98-001-12





LLNL's first "nuclear" test was designed on the UNIVAC and slide rules



LLNL was less than one year old

- The device was placed on a 300foot tower and the physicists stood far away, observing with dark glasses
- Upon detonation, only a small cloud of dust appeared
- When the dust cleared, the tower was still standing

Nowhere to go but up ... and 50 years later, the ASCI program

NS-98-031. 1

During design-test-build, our simulation codes normalized complex phenomena against test data





- Computers lacked speed and memory to run full problems
- Some nonlinear physical processes not understood
- Nuclear test data provided normalizing factors to make simulations accurate
- Normalization factors differed from system to system







		L	LNL	Com	pute	r Hist	ory				
				Year							
52 53 54	55 56 57 58 59	លែជឧខស	65 66 87 83 69	70 71 72 73 74	75 76 77 73 79	30 31 32 30 34	35 36 37 32 39	90 91 92 93 94	95 96 97 93 99	-	10000000
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The computational needs of the SSP span many time and length scales





























Achieving the 100-teraFLOPS milestone will require carefully integrated efforts to develop unprecedented computer platforms, high-fidelity physics codes, and a world-class computing environment.







IBM

NS-88-031. 25

The SSP announced strategic academic alliances with five universities

- Stanford University
 - The Center for Integrated Turbulence Simulations
 - William C. Reynolds (wcr@thermo.stanford.edu)
- The University of Chicago
 - Astrophysical Thermonuclear Flashes
 - Robert Rosner (rrosner@oddjob.uchicago.edu)
- The University of Illinois an Champaigne, Urbana
 - Center for Simulation of Advanced Rockets
 Michael T. Heath (m-heath@uiuc.edu)
- The University of Utah
 - Center for Simulation of Accidental Fires and Explosions
 - David W. Pershing (David.Pershing@dean.eng.utah.edu)
- The California Institute of Technology
 - Facility for Simulating the Dynamic Response of Materials
 - Daniel I. Meiron (dim@ama.caltech.edu)







ASCI is an essential part of the rapidly evolving Stockpile Stewardship Program

- ASCI provides leading-edge, high-end simulation capabilities to meet weapon certification requirements
- ASCI integrates the resources of national laboratories, computer manufacturers, and academic institutions
 - national labs focus on application codes and related applied science
 - computer manufacturers develop technology and systems for 100 TeraFlops
 - Academic institutions research the basic science

The ASCI codes will need to be continually evaluated against experimental data in the relevant regimes







Our future certification of the stockpile will rely on informed judgments

- Trained, knowledgeable people are required to assess and certify the stockpile
- A deeper understanding of the underlying science is required for practical weapon assessment capabilities
- New computational capabilities are needed to provide the integration formerly done with nuclear tests
- New experimental capabilities are required to provide detailed component level tests and validate the computation tools



Full implementation of SSP is required to sustain nuclear deterrence

NS-98-411, 39

There are many risks inherent in the SSP



- NASA did not accept the judgment of its engineers that the design was unacceptable and,
- As the problems grew in number and severity, NASA minimized them in management briefings and reports.
 - Reports of the Presidential Commission on the Challenger accident

"The contractor did not accept the implications of tests early in the program that the design had a serious and unanticipated flaw





















































































































































