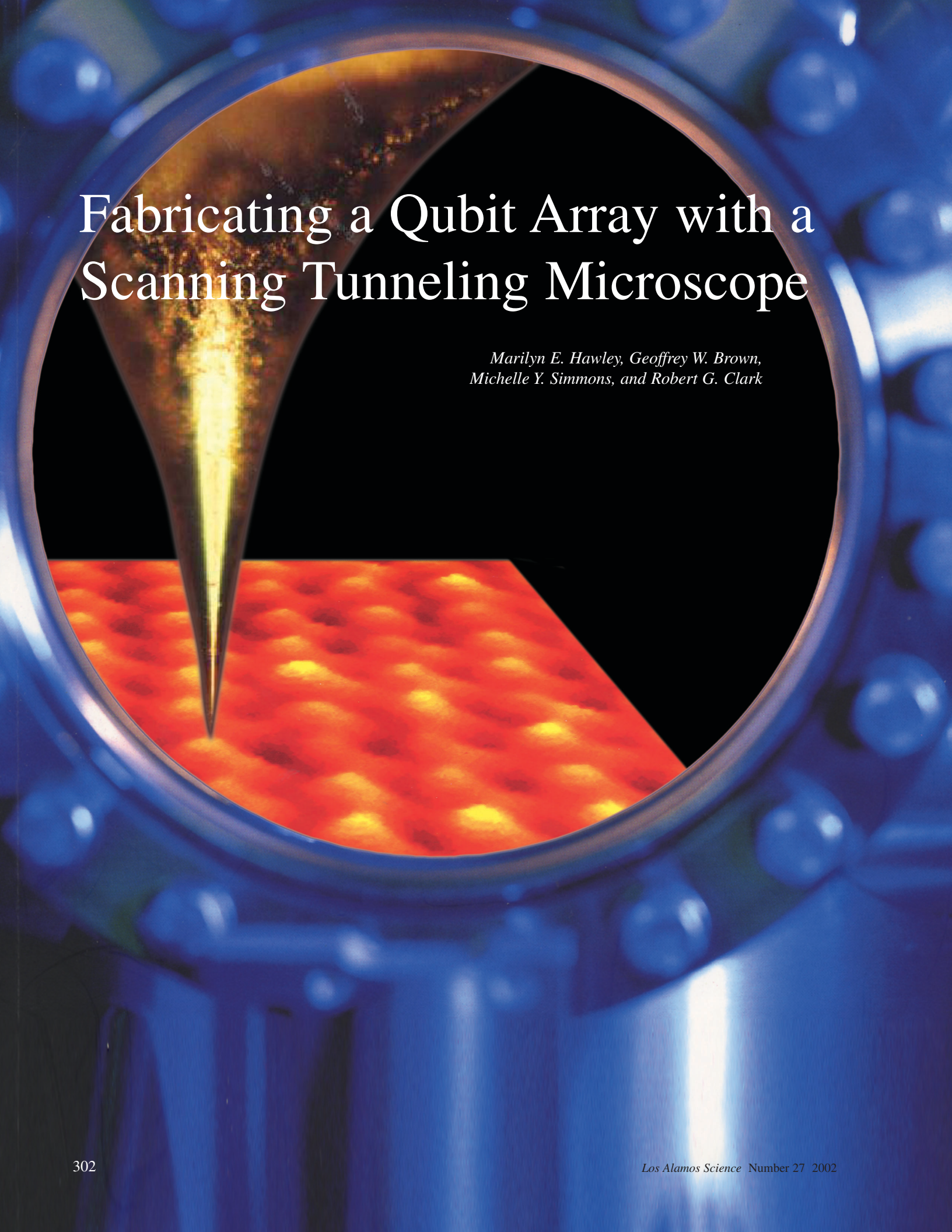

Fabricating a Qubit Array with a Scanning Tunneling Microscope

Marilyn E. Hawley, Geoffrey W. Brown, Michelle Y. Simmons, and Robert G. Clark

The Australian Centre for Quantum Computer Technology and Los Alamos National Laboratory are working together to answer the question, "Can the solid-state quantum computer (SSQC) proposed by Bruce Kane (1998) be built?" Illustrated in Figure 1, the architecture put forward by Kane requires a linear array of phosphorus atoms (nuclear spin 1/2) inside an isotopically pure silicon-28 (spin 0) wafer. The spacing between the atoms needs to be about 20 nanometers, and the array will be located 5 to 20 nanometers beneath the silicon surface. An array of metal electrodes, isolated from the silicon by a thin insulating layer of silicon dioxide (SiO_2), will sit above the qubit array and needs to be precisely registered to it. Because the array is so small and because the silicon overlayer must be nearly free of impurities and crystalline defects for the computer to operate properly, we must achieve unprecedented control of the fabrication process.

Our efforts to build the SSQC focus on a novel "bottom-up" fabrication approach. Starting with a clean silicon surface, we will build each layer of the device in succession, first creating the phosphorus array and embedding it in the surface, then growing the silicon overlayer, the SiO_2 insulating layer, and finally laying down the metal electrodes. (We are also pursuing a "top-down" fabrication approach, which along with information about the operating principles of the computer, is described in the article "Toward a Silicon-Based Nuclear-Spin Quantum Computer" on page 284.)

The scanning tunneling microscope (STM) plays a central role in the bottom-up approach, serving as both a fabrication and electrical characterization tool. To create the phosphorus array, we employ STM-based hydrogen lithography, developed by Joseph Lyding's group at the University of Illinois at Urbana-Champaign (Lyding et al. 1994). Immediately following the array fabrication step, the silicon overlayer will be grown by molecular beam epitaxy to encapsulate the array. Our STMs have variable temperature control so that we can anneal the overlayer in situ, and thus be in a position to study the stability of the phosphorus array during silicon overgrowth. We can also identify potential defects and impurities that could impair computer operation. Once the thin SiO_2 layer is grown, we will create the metal-gate array using state-of-the-art electron beam lithography (EBL) technology.

In this article, we summarize our progress in building the phosphorus array, overgrowing the silicon layer, and checking whether the latter step alters the array. To convey the central role of the STM in building the SSQC, we start by presenting the principles that make it such a powerful fabrication and characterization tool.

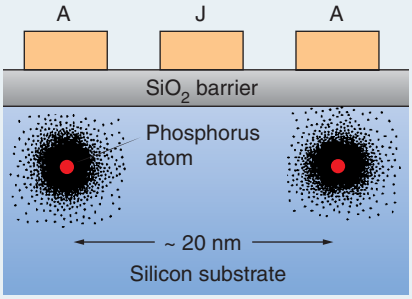

Figure 1. Kane's Architecture for a Quantum Computer
In Kane's concept of a silicon-based quantum computer, the qubits are phosphorus atoms embedded in an isotopically pure ^{28}Si crystal at a distance of about 20 nm from each other. Above the silicon, there is an insulating barrier of SiO_2, and above that barrier, metallic gate electrodes. The A-gates help manipulate the individual qubits whereas the J-gates control the interaction between neighboring qubits.

Scanning Tunneling Microscopy

The STM probes the surface of a sample by inducing electrons to tunnel between the surface and the tip. As illustrated in Figure 2, an extremely sharp metallic tip (with radius of curvature R that is typically about 10 nanometers) is brought to within a few angstroms of a sample's surface. The thin vacuum region separating the tip and the sample forms a potential barrier, and a bias voltage between the tip and the sample causes more electrons to tunnel through the barrier from occupied energy states to unoccupied ones. To a first approximation, the tunneling current at a point on the surface is proportional to the local electron density of states (LDOS) in the sample. By measuring the tunneling current as a function of position, we can obtain an extremely localized map of the electronic structure of the sample's surface.

The tip is attached to a piezoelectric scanning device, which moves it over the surface of the sample in a raster pattern. An image of the surface is thus obtained. In practice, we use a feedback loop to adjust the tip height and keep the tunneling current constant as the tip moves. (Scanning in this "constant-current" mode prevents the tip from crashing into protrusions, such as surface steps.) The resulting map of tip heights versus position can be used to construct an image of the surface that shows contours of constant LDOS. On many surfaces, this

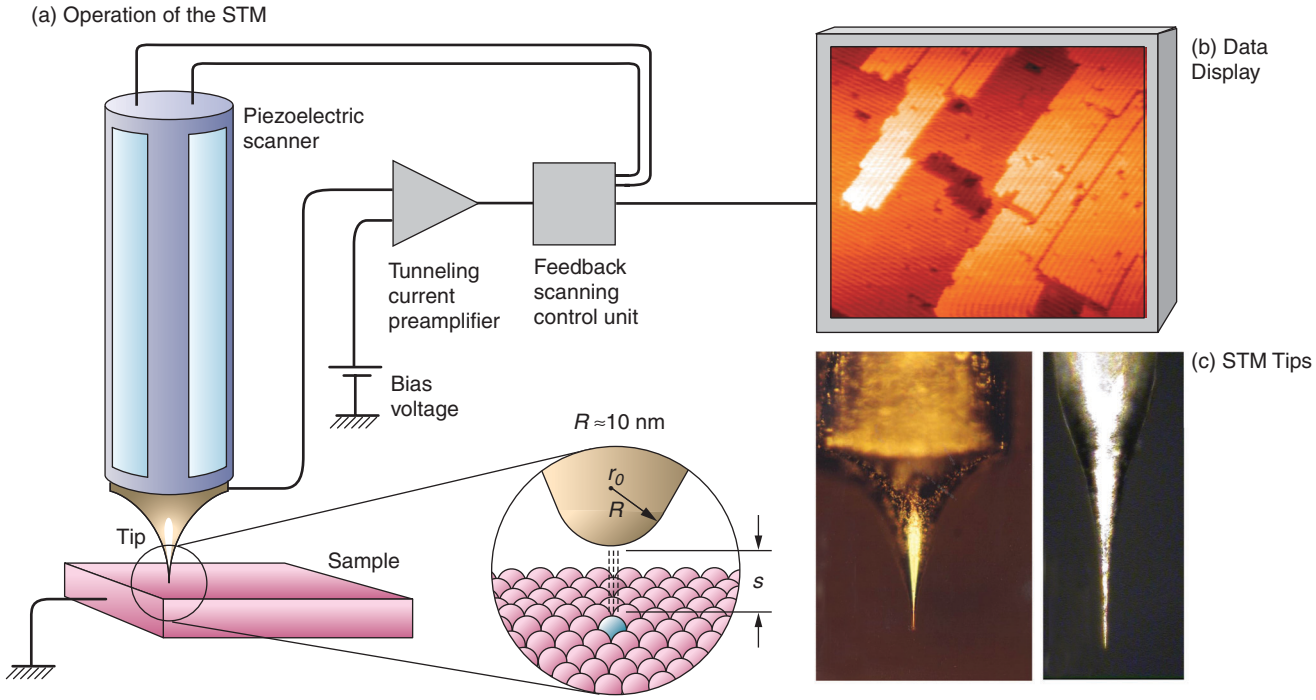

Figure 2. The Scanning Tunneling Microscope (STM)
(a) This schematic diagram illustrates the steps in the operation of an STM. An extremely sharp tip is held within a few tenths of a nanometer of a sample surface. A bias voltage *V* applied between the tip and the sample causes electrons to tunnel between the two. The tunneling current is monitored with a feedback loop, which keeps the current constant by varying the gap width *s* between the tip and the sample. The gap width is then proportional to the sample's local density of states (LDOS). The tip moves in a raster pattern laterally over the surface. A plot of the tunneling current versus position is a map of the sample's LDOS. One such map is shown in (b). In many cases it is equivalent to a map of atomic positions. (c) These optical micrographs show two STM tips: One is made of tungsten (left) and the other, of etched 90% Pt–10% Ir alloy. Each tip has a radius of curvature of about 10 nm.

contour map is equivalent to a map of the atomic positions.

The electronic-energy diagrams of the tunneling process, shown in Figure 3, help to explain the technique's atomic resolution, as well as the subtleties of the information obtained. The applied bias voltage defines the energy offset, or energy "window," between the Fermi levels of the tip and the sample. Any electrons that have energies within that window contribute to the net tunneling current.

In 1985, shortly after the development of the STM, Jerry Tersoff and Donald Hamann described the tunneling mathematically, by applying Bardeen's tunneling theory (1961) to the tip-sample system. By assuming a low temperature, a small bias voltage V, and a featureless tip (one in which the electron density of states is constant), they showed that the tunneling current could be written as

$$I_t \propto \sum_{\nu} \left|\Psi_\nu(r_0)\right|^2 \delta\left(eV - E_F\right) \quad . \qquad (1)$$

Here, Ψ_ν are the sample's wave functions whose energy eV above the Fermi level E_F is evaluated at the point r_0 on the tip—see Figure 2(a). The sum over the probability densities from all such wave functions is the LDOS of the sample directly below the tip, so that in the approximation of Equation (1), the tunneling current is indeed proportional to the sample's LDOS.

The spatial resolution of an STM image is extremely high (approximately 0.01 angstrom) in the direction perpendicular to the surface. That is so because the tunneling probability T decreases exponentially with the separation s between the tip and the sample. The Wentzel-Kramers-Brillouin (WKB) approximation for the tunneling probability through the type of potential barrier shown in Figure 3 (a trapezoidal barrier between planar metal electrodes) yields

$$T = e^{-2\kappa s} \quad , \qquad (2)$$

where κ, the inverse decay constant in the potential barrier, is given by

$$\kappa = \sqrt{\frac{2m_e}{\hbar^2}\left(\frac{\phi_t + \phi_s - eV}{2} - E\right)} \quad . \qquad (3)$$

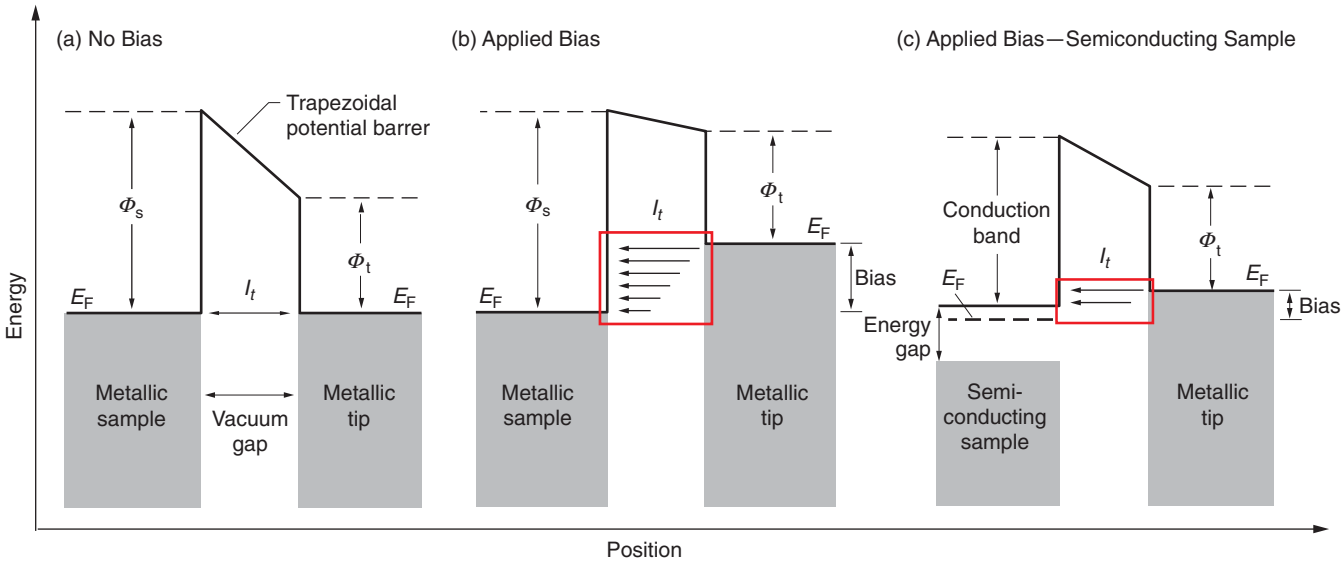

Figure 3. Tunneling Process for Metallic and Semiconducting Samples

This schematic electronic-energy level diagram helps illustrate basic STM concepts. Filled electronic states are below the Fermi level E_F whereas empty states are above. A potential barrier is created by the vacuum gap between the tip and sample. If the width of the barrier is so narrow that the electron wave functions of the tip and sample overlap, then electrons can tunnel to empty states in either the tip or the sample. (a) When the two Fermi levels are equal (because the tip and sample are connected to a common ground) there is no net current flow. (b) When a bias voltage is applied, the Fermi levels of the two materials become unequal, and the difference defines an energy window (red box). In the case shown, the bias voltage raises the Fermi level in the metal tip relative to that in the metal sample. Electrons in filled states within the energy window can tunnel from the tip, through the potential barrier, into the sample's empty states. The arrows of decreasing size indicate that the tunneling probability is highest for electrons at the Fermi level of the tip and decreases as the electron energy decreases. (c) No states are available in the energy gap between filled states and the conduction band of a semiconductor sample. Electrons can only tunnel into empty states in the conduction band.

In Equation (3), m_e is the free-electron mass in vacuum, and $\hbar$ is the reduced Planck constant. The variables are the work functions[1] of the tip and the sample, ϕ_t and ϕ_s, respectively, the electron kinetic energy normal to the barrier E (measured relative to the tip's Fermi level), and the bias voltage V applied to the sample.

Given nominal values for the parameters in Equation (3) (for example, $\phi_t \approx \phi_s$ = 3–6 electron volts, $E \approx 0.025$ electron volts, and V = 1–2 volts), the decay constant κ is of the order of 0.1 nanometer^{-1}. A change of 0.1 nanometer in the spacing between the tip and the sample alters the tunneling probability by $e^2 = 7.4$. Thus, a topographic resolution of the order of 0.001 nanometer in the direction perpendicular to the surface requires only a 2 percent precision in the measurement of the tunneling current. With carefully designed, low-noise electronics, that precision is easily achieved—even for a tunneling current of 100 picoamperes.

The resolution parallel to the surface is also atomic—on the order of 0.1 nanometer—for much the same reason: The extreme sensitivity of the tunneling current to the gap width ensures that essentially the entire tunneling current arises from a single atom or a small cluster of atoms at the very end of the tip (those atom(s) closest to the sample). On a clean, well-formed tip with a small radius of curvature, atoms or clusters that are laterally displaced from the end are also farther from the sample and do not contribute a significant number of electrons to the tunneling current. Thus, there is very little lateral spread associated with the signal.

A more-detailed look at the origin of the tunneling current will shed additional light on the information contained in the STM image. Equation (1) can be rewritten to account for both a finite energy window for tunneling and a more-complex electronic structure of the tip as follows (Selloni 1985):

$$I_t \propto \int_{-eV}^{0} \rho_t(E)\ \rho_s(E+eV)\ T(E,eV)\, dE\,, \quad (4)$$

where ρ_t and ρ_s are the tip and sample LDOS, respectively, T is the tunneling probability between the tip and the

[1] The work function ϕ is the energy needed to remove an electron, whose energy is at the Fermi level, from the sample.

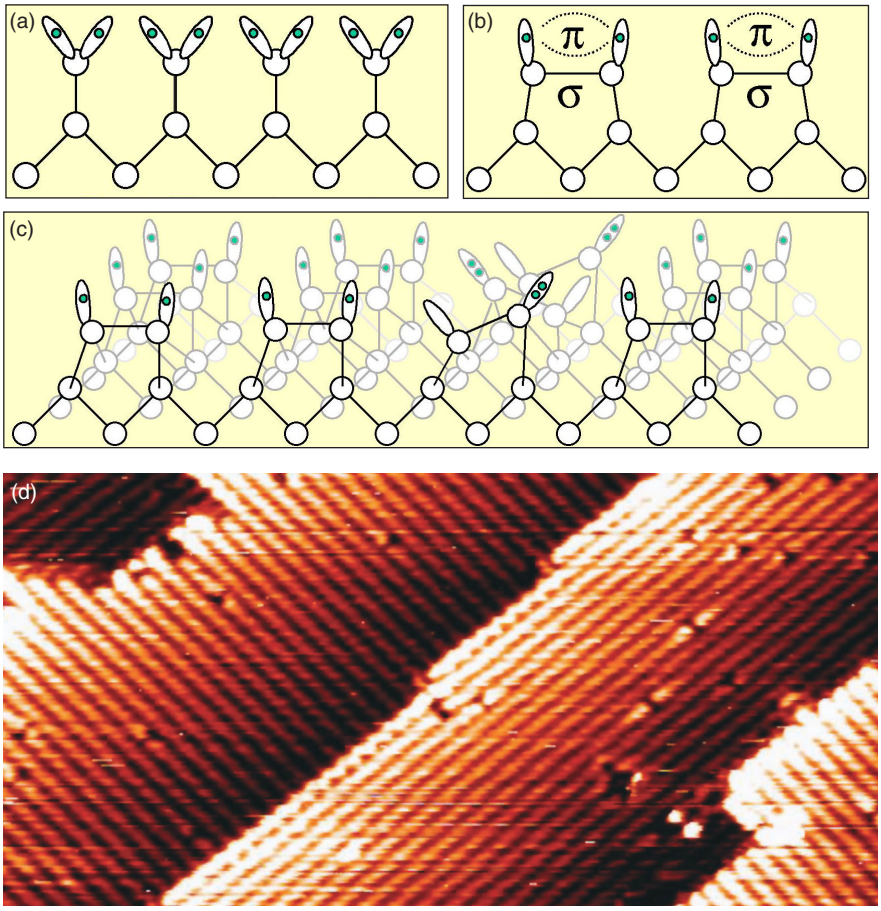

Figure 4. The Si(100)-(2 × 1) Surface
(a) Schematic view of a row of atoms in a bulk-terminated Si(100) surface. This configuration is energetically unfavorable because every atom has two singly occupied dangling bonds. (b) The bulk-terminated surface can reconstruct into the so-called Si(100)-(2 × 1) surface. The dangling bonds of neighboring atoms join to form σ-bonded dimers, and the remaining protruding bonds become weakly π-bonded. (c) This view of the reconstructed surface shows several rows of dimers. In the third row from the left, the dimers are pinned in the buckled configuration (see text). (d) A filled-state image of a Si(100)-(2 × 1) surface (10 nm × 5 nm) showing several monolayers. The bright lines making up each "terrace" are the dimer rows, which rotate by 90° with each successive layer. The defect density of an average sample is approximately 5%. The wavy line along the upper edge of the central terrace is due to buckled dimers.

sample, and the dependence of the tunneling current on r_0 has been suppressed for simplicity.

The expression in Equation (4) emphasizes that the properties of both the tip and the sample contribute to the tunneling current. Therefore, one needs to have substantial background information about both in order to interpret an STM image. For example, numerous geometric and electronic effects go into the LDOS function ρ_s, including the electronic structure at the surface, the band structure of the material, the presence of dangling bonds at the surface or bulk resonances, the number and orientation of back bonds, and so forth. In addition, we need information about the electronic structure of any adatoms or contaminants (such as oxygen, carbon, carbon dioxide, nitrogen, and others) that might be present. Through ρ_t, the appearance of an image is also closely related to the electronic structure of the tip. Finally, of particular importance is the fact that the electron density is not always centered about the cores of the atoms in the material. Several of these considerations arise in our work on the SSQC and will be discussed later.

One powerful technique that can be used to help us interpret images is to change the direction (sign) of the bias voltage. By doing so, we cause the tunneling current to reverse its direction. If the tip is biased to have a higher Fermi level, then current flows from the tip to the empty states in the sample. If the bias is reversed, so that the sample has a higher Fermi level, then the electrons from the sample's filled states flow into the empty states in the tip. We therefore have a means to obtain information about the density of both the empty and filled states of the sample. The differences between the two STM images help us sort out electronic effects from structural information and to distinguish among features that appear identical when only one bias direction is used.

Despite the intricacies involved, we can interpret an STM image quite accurately when all the available information is taken into account. That is why STM imaging is continuing to produce significant results in surface science.

Preparing Silicon(100) Surfaces

The bottom-up fabrication approach begins by preparing a flat (100)-oriented silicon surface. Technologically, this is one of the most important semiconductor surfaces. For our purposes, it is relatively easy to prepare, can be patterned by

STM-based hydrogen lithography, and is well suited for the subsequent overgrowth of crystalline silicon layers. Although the (100) surface has been studied by STM and other methods for over 15 years, we are uncovering new details important to constructing the type of atomic-scale electronic structures needed in the Kane solid-state quantum computer and other quantum devices.

Figures 4(a) and 4(b) show how the bulk-terminated (100) surface, every atom of which has two dangling bonds, reconstructs in a manner that lowers the surface energy. Electrons from two neighboring silicon atoms form a σ-bond, so the resulting silicon-silicon dimer has only two dangling bonds. These bonds form a weak π-bond to further reduce the surface energy. The π-bond can easily be broken by chemically active species, such as hydrogen, which adsorb on the surface.

The reconstructed surface, commonly referred to as the Si(100)-(2 × 1) surface (a designation that derives from the corresponding electron-diffraction pattern), takes on the appearance of a neatly plowed field, with rows of dimers aligned parallel to each other, as seen in Figures 4(c) and 4(d). In filled-state STM images taken at room temperature, most of the dimers appear as symmetric bean shapes. In reality, the dimers are tilted, or buckled, and are flipping back and forth between buckled configurations very rapidly—refer to Figure 4(c). The oscillation takes place too quickly to be imaged with an STM. Therefore, in general, an average configuration is observed. Near defects or step edges, however, the dimer can be pinned in an asymmetric position and imaged. Such an image can be seen at several locations in Figure 4(d), where neighboring dimers are seen to buckle in alternate directions.

Surface preparation begins with degassing the sample and its holder by holding them at an elevated temperature for several hours. (Because the surface is reactive, this step and those that follow are carried out in ultrahigh vacuum.) The sample is flash-heated to a temperature of 1250°C and cooled under conditions that allow the surface silicon atoms to form a well-ordered Si(100)-(2 × 1) surface. But the difficulty in precisely controlling the annealing process and the inability to cut the starting substrate exactly on axis result in a surface typically consisting of several terraces of simple atomic planes. On a given terrace, all the dimer rows run in the same direction, whereas the in-plane orientation of the dimer rows rotates by 90° from one terrace to the next. The terrace edges terminate smoothly or roughly, depending on whether the dimer rows for that terrace run parallel or perpendicular to the terrace edges, respectively.

Even a freshly prepared Si(100)-(2 × 1) surface will contain defects. The main types observed in STM images, illustrated in Figure 5, are type A defects, in which a single silicon dimer is missing, type B, in which two adjacent dimers in a row are missing, and type C, whose make-up is still controversial. Type C defects could be the result of a subsurface vacancy, or else consist of two missing silicon atoms from adjacent dimers in a row. They could also be due to an adsorbed impurity, for example an absorbed water molecule (Chander et al. 1993). Although it is nearly impos-

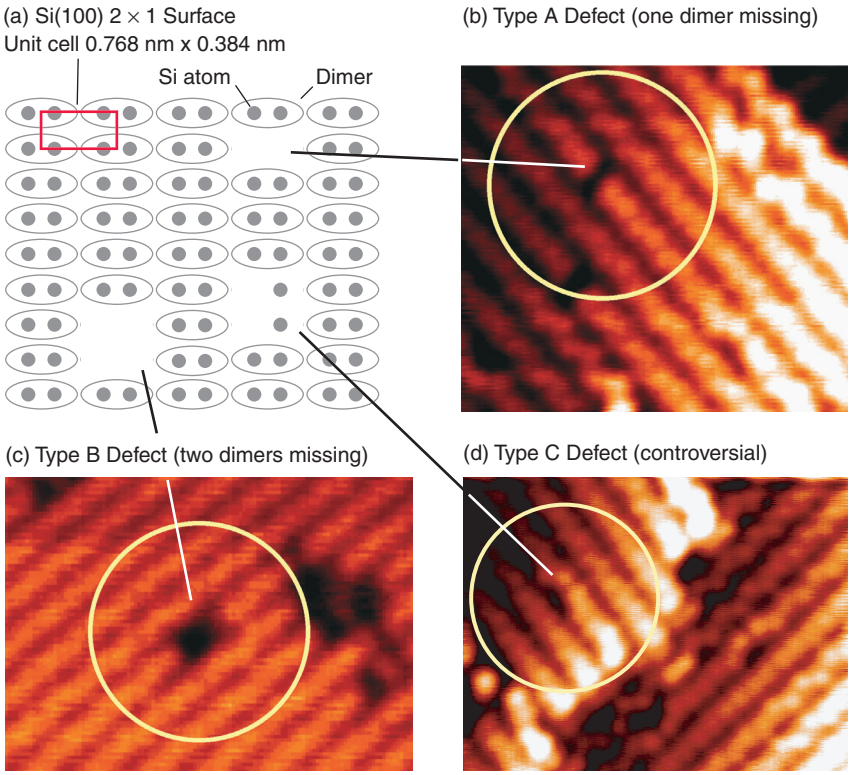

Figure 5. Defects in the Si(100)-(2 × 1) Surface
(a) This cartoon of the Si(100)-(2 × 1) surface illustrates type A, B, and C defects. (The structure of a type C defect is controversial. See text for a further discussion.) The 0.768 nm × 0.384 nm unit cell (the values are for the dimer spacings along the rows and between the rows, respectively) is also shown. (b), (c), and (d) show filled-state images of type A, B, and C defects, respectively.

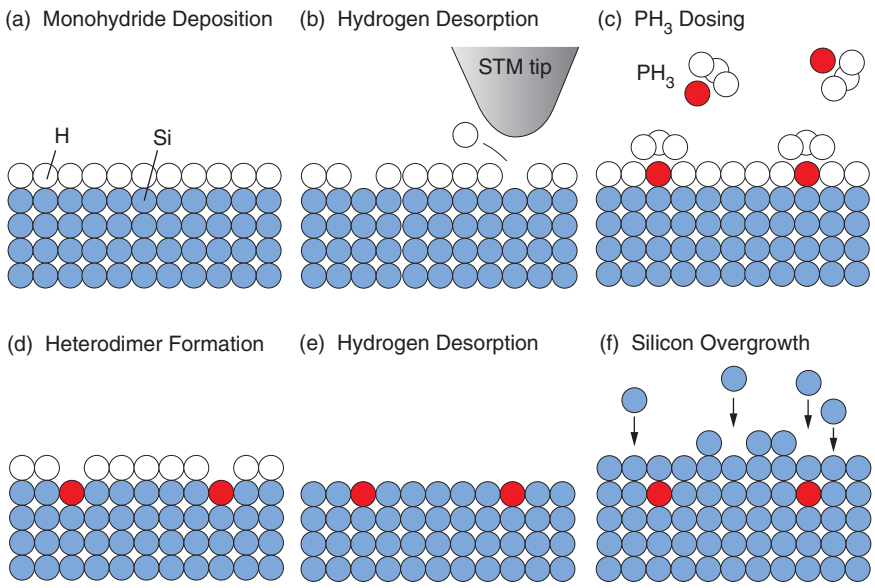

Figure 6. The Bottom-up Approach for Fabricating an Array of Phosphorus Qubits
(a) After preparing and cleaning a silicon surface, we dose it with hydrogen, which adsorbs as a monoatomic layer. (b) The STM tip selectively desorbs individual hydrogen atoms and exposes silicon at a set of regularly spaced sites that will define the qubit array. (c) PH_3 is introduced into the vacuum chamber. It bonds to the silicon only at the exposed sites. (d) A critical anneal is performed to incorporate the phosphorus atoms into the silicon surface, forming a P-Si heterodimer. (e) The hydrogen monolayer can be removed by further annealing at a slightly higher temperature (this step may not be necessary). (e) With molecular-beam epitaxy, the phosphorus array is buried under fresh layers of silicon.

sible to eliminate these defects during preparation, we can prepare surfaces with defect densities of less than a few percent by following careful vacuum practices in the STM chamber. The effect of defects on the operation of a quantum computer will be further discussed under the section "Qubits, Defects, and Dopants."

STM-Based Hydrogen Lithography

Once we have prepared a clean surface with a low defect density, we are ready to begin the array fabrication scheme. We use a resist technology analogous to the lithographic techniques used in conventional electronics manufacturing, the main difference being that the STM-based technology allows us to create features on the atomic scale.[2] The idea is illustrated in Figure 6.

The first step is to deposit a single layer of hydrogen atoms (the "resist") on the clean surface. In order to do so, we dissociate molecular hydrogen gas by passing it over a hot filament as it enters the STM vacuum chamber. The resulting hydrogen atoms are directed onto the heated sample surface, where they break the weak π-bond and adsorb to the surface by attaching to the very reactive dangling bonds. Provided the conditions are right, one hydrogen atom can covalently bond to each silicon atom, and the surface becomes coated with a uniform monohydride layer (see Figure 7).

The STM tip is then used as the lithographic patterning tool. Controlled-voltage pulses applied between the tip and the sample cause very small patches of the monohydride layer to vibrate and heat up and/or to become electronically excited. Individual hydrogen atoms are liberated, and as a result, the dangling bond of the underlying silicon atom becomes exposed. The tiny, atom-sized holes created by the STM are the only reactive sites on the otherwise unreactive monohydride layer. Interestingly, the holes created in the hydrogen layer appear as protrusions above the hydrogen-terminated surface. This is an example of electronic effects influencing the STM images. Whereas the hydrogen-terminated structures protrude farther into the vacuum than the dangling bonds, the energy of the dangling bonds is closer to the window between the Fermi levels of the tip and the sample. The dangling bonds, therefore, contribute more strongly to the tunneling current and appear "taller."

Next, we introduce high-purity phosphine (PH_3) gas directly into the ultrahigh-vacuum chamber of the microscope. The PH_3 is very reactive and adheres to the exposed dangling bond with a sticking coefficient of one. As seen in Figure 8, we can place single phosphorus-bearing molecules where necessary and thereby build an atomic-scale phosphorus array. The reacted sites appear taller than both the hydrogen-terminated sites and the unreacted dangling bonds. This effect is likely due to a combination of electronic and physical effects.

The next step is to stimulate the phosphorus atoms within the phosphine molecule (which is attached to the silicon atoms by a single bond) to

[2] Scanning tunneling microscopy can be used directly to create atomically precise structures of metal atoms on metal surfaces. We are forced to adopt a lithography approach because the strong covalent bonds on the silicon surface prevent us from directly rearranging atoms using the STM.

incorporate into the top layer of the silicon surface and form a phosphorus-silicon heterodimer. In that structure, the phosphorus atom takes the place of one of the silicon atoms in the dimer and attaches to the remaining silicon surface through three strong covalent bonds. Formation of the heterodimer is a critical step because it secures the phosphorus atom in its patterned location and helps prevent its diffusion during subsequent processing steps.

Before studying the mechanism for incorporation through the hydrogen resist, we had to learn how to distinguish the postdosing phosphorus-related species from other features on the silicon surface because, to date, very few reports exist on the STM imaging of single phosphine molecules on silicon. We, therefore, conducted a series of experiments in which the clean Si(100)-(2 × 1) surface was subjected to various dosing conditions. Each time, the presence of phosphorus on the surfaces was confirmed by Auger electron spectroscopy. By examining both filled- and empty-state STM images, we found it was possible to distinguish between phosphine-related surface species and surface defects.

We then faced the challenge of phosphorus incorporation. It is well known that, at room temperature, phosphine adsorbs onto a clean Si(100)-(2 × 1) surface and quickly dissociates to form PH_2 and H. Subsequent heating of the surface to about 400ºC leads to the complete dissociation of PH_x (x = 2–3). We have demonstrated that, at these temperatures, the individual phosphorus atoms also incorporate into the surface and form the phosphorus-silicon heterodimer (see Figure 9). The hydrogen remains on the surface as a monohydride. Continued heating of the surface to higher temperatures will liberate the hydrogen. In this way, the surface is left clean, consisting of only silicon dimers and phosphorus-silicon heterodimers.

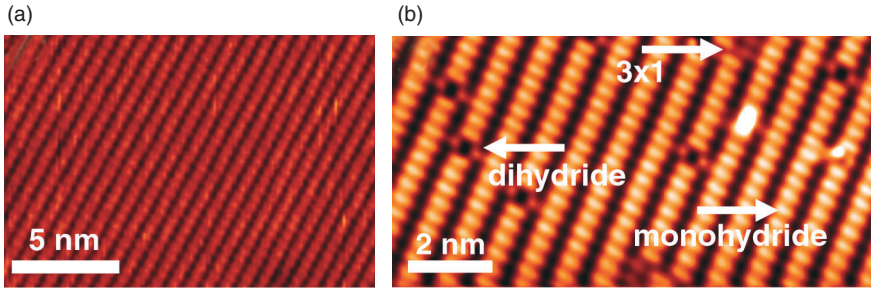

Figure 7. Creating the Hydrogen Resist
(a) This filled-state STM image is of a clean Si(100)-(2 × 1) surface with a very low defect density. (b) Shown here is a hydrogen-terminated Si(100)-(2 × 1) surface, which is almost entirely monohydride; that is, one hydrogen atom is bonded to each silicon atom. Several other structures are also apparent: dihydrides (two hydrogen atoms have bonded to a single silicon atom) and a 3 × 1 structure (three hydrogen atoms have bonded to one silicon atom).

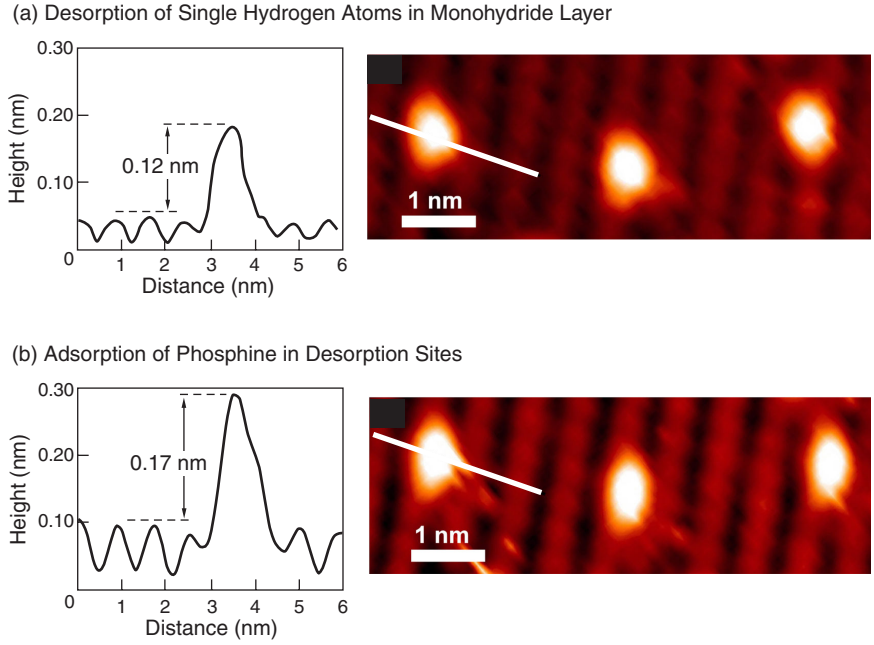

Figure 8. Adsorption of Single Phosphine Molecules
(a) This STM image (right) shows three desorption sites in a monohydride layer, and the graph (left) shows the line profile, taken along the indicated white line, of the leftmost site. The bright protrusion at each of the desorption sites is the signature of the single silicon dangling bond after desorption of just one hydrogen atom. (The sites appear brighter because their DOS are closer to the Fermi level, so they contribute more to the tunneling current.) (b) The same sites after dosing the surface with phosphine gas. The profile shows an increase of 0.05 nm in height (calibrated against an atomic step edge on the same surface), a reproducible increase that is observed at all adsorption sites. Given the information we gathered by scanning tunneling microscopy, our interpretation of the increase in height is that phosphine has adsorbed to the exposed sites.

Molecular Beam Epitaxy of Silicon

Subsequent steps for the fabrication of the SSQC call for growing a 50- to 200-angstrom-thick layer of crystalline silicon over the array of phosphorus atoms, depositing an insulating layer of SiO_2, and aligning gate electrodes to the now buried phosphorus array. High-quality crystalline, or epitaxial, growth of silicon on silicon is typically done at high temperatures.

However, it is known that at high temperatures, phosphorus atoms buried in silicon tend to diffuse upwards and pop up to the surface. Furthermore, we observed during our incorporation studies that, at temperatures of 650ºC and above, the phosphorus becomes mobile. It breaks from the heterodimer and begins to migrate about the surface until it meets another phosphorus atom. It then forms P_2 (or possibly P_4), which desorbs from the surface. Thus, the next significant question in the bottom-up approach is, "Can crystalline silicon be grown on either a clean or monohydrided surface at temperatures low enough to prevent the diffusion and segregation of phosphorus?"

Taking into account results from the literature and our own experiments, we have adopted two parallel growth strategies. We begin both by annealing the sample directly after phosphine dosing, so that the phosphorus atoms become incorporated into the silicon surface and the hydrogen resist can desorb. We then need to encapsulate the phosphorus atoms under a few monolayers of silicon. In the first growth strategy, we will grow the encapsulation layer at room temperature. The resulting layer will have a high surface roughness with numerous silicon islands and require a subsequent annealing step for surface flattening. In the second strategy, we

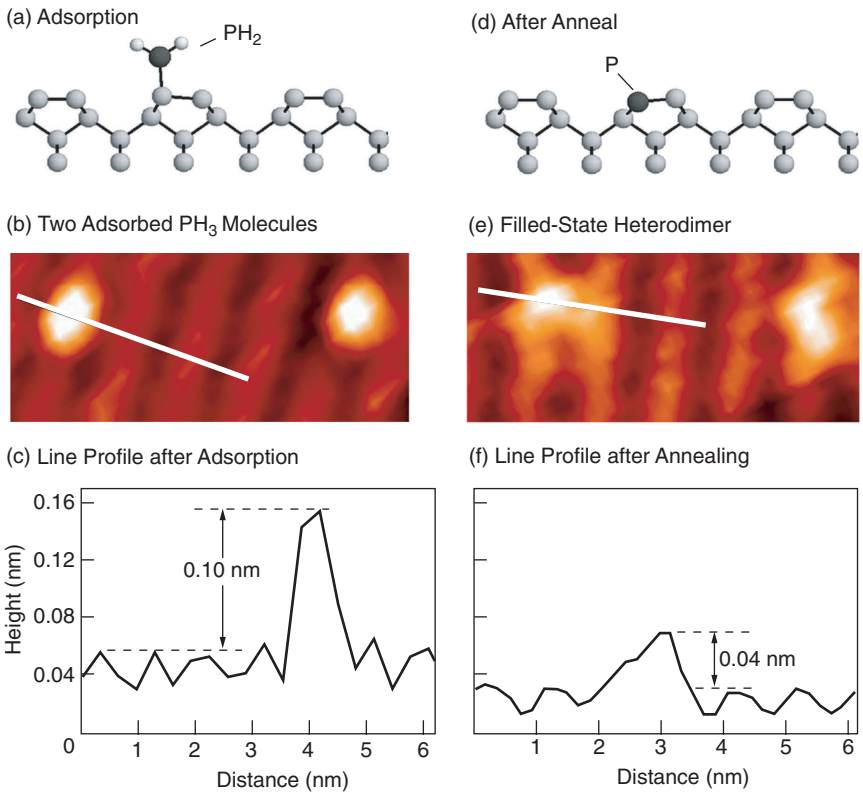

Figure 9. Incorporation of Phosphorus into the Surface
(a) This schematic diagram illustrates how phosphine molecules adsorb onto the bare Si(100)-(2 × 1) surface. The filled-state STM image in (b) is of a pair of adsorbed phosphine molecules, and (c) shows the line profile through the left molecule. (d) After annealing the surface to 400°C, the phosphorus atom incorporates into the silicon surface and forms a Si-P heterodimer. (e)–(f) These figures show the filled-state STM image of the heterodimer and the corresponding line profile. A comparison between (c) and (f) shows that there is a characteristic height difference between the nonincorporated and incorporated phosphorus, the former extending higher above the surface plane.

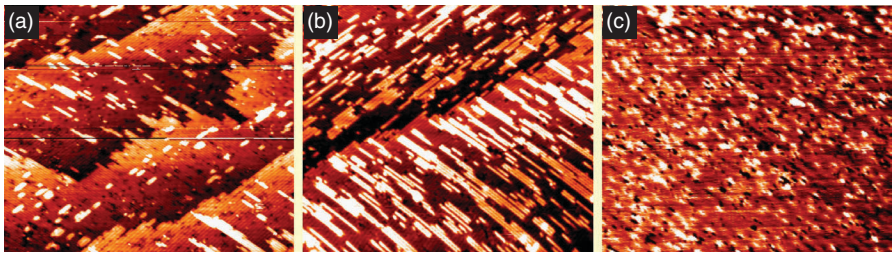

Figure 10. Images of Different Silicon Coverages
These images (100 nm × 85 nm) of a Si(100)-(2 × 1) surface show different stages of epitaxial silicon growth. The silicon was deposited while the sample remained in the microscope and was held at about 250°C. (a) The sample is shown after a 0.08 monolayer was grown. Epitaxial growth is demonstrated by the elongated shape of the islands and their direction being perpendicular to the underlying dimer rows. (b)–(c) The sample is shown after a deposition of 0.5 monolayer and a complete monolayer, respectively. At the growth temperature noted above, the surface is rough. Defects and silicon vacancies dominate the topography.

will try to grow the silicon at an elevated temperature. Because the layers will grow epitaxially, we can eliminate the subsequent anneal, but the challenge will be to find a growth temperature that also minimizes the segregation and diffusion of the phosphorus atoms.

A significant number of experiments need to be conducted to determine the optimal encapsulation conditions. By integrating a small silicon evaporator into the STM chamber, we have already begun to study the epitaxial deposition of thin silicon layers at low temperatures. Figure 10 shows growth in the thickness of silicon of up to one monolayer at 250°C. The new layer grows epitaxially. Before it is annealed, the complete monolayer still exhibits vacancies that are not filled during the silicon overgrowth. Their possible detrimental effects on the operation of the quantum computer will have to be evaluated.

We have also begun to explore the first growth strategy (see Figure 11). We incorporated phosphorus into the silicon surface, deposited a few monolayers of silicon at room temperature, then annealed the sample for 1 minute at 250°C. As seen in Figure 11(b), this surface was fairly coarse and not suitable for subsequent epitaxial growth. A flat surface structure with island-free terraces was observed only after the sample had been annealed at 600ºC. Figure 11(c), however, shows that, at those elevated temperatures, the phosphorus atoms have diffused to the surface. Although that result is disappointing, we are not discouraged. Ours are the first such studies of phosphorus encapsulation and silicon overgrowth. The preliminary results simply demand that we look for a new way to obtain a flat surface at lower annealing temperatures or an alternative way to inhibit phosphorus diffusion.

We have, however, settled the question of whether the incorporated phosphorus atoms are electrically active, that is, whether their donor electrons are free to conduct. We first grew a thin layer of phosphorus on a silicon substrate and buried it under a thick silicon layer (grown at the relatively low growth temperature of 250°C), creating a so-called delta-doped layer. According to the literature, our growth and annealing conditions resulted in a two-dimensional (2-D) density of 1.7×10^{14} phosphorus atoms per centimeter squared. If each atom is electrically active, it would contribute one free electron to the substrate. When we measured the electron density through the Hall effect at a sample temperature of 4 kelvins, the result was a 2-D density of 2.0×10^{14} electrons per centimeter squared (see Figure 12). As the two numbers agree within measurement errors, it seems that all the phosphorus atoms are electrically active (Oberbeck et al. 2002). This result suggests that the phosphorus atoms

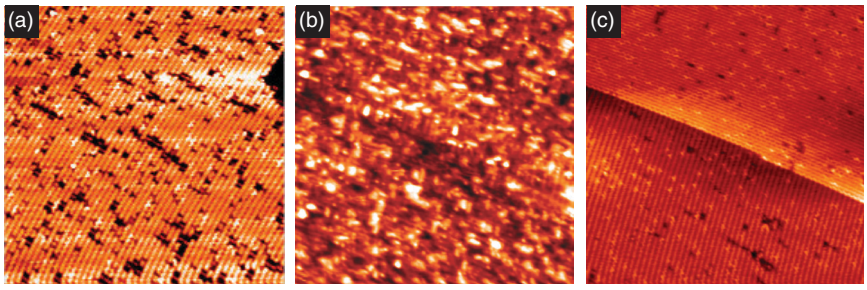

Figure 11. Silicon Overgrowth and Annealing after Low PH_3 Dosing
(a) A Si(100)-(2 × 1) surface is shown after low PH_3 dosing and annealing to incorporate phosphorus atoms into the Si-P heterodimers. The heterodimers are visible as bright zigzag structures. The image size is 50 × 50 nm². (b) The epitaxially overgrown surface is shown after annealing at 250°C. The image size is also 50 × 50 nm². The surface is too coarse for the SSQC and must be annealed. (c) After annealing at 600°C, the surface is flat. The bright spots indicate, however, that phosphorus has diffused to the surface. The image size is 55 × 55 nm².

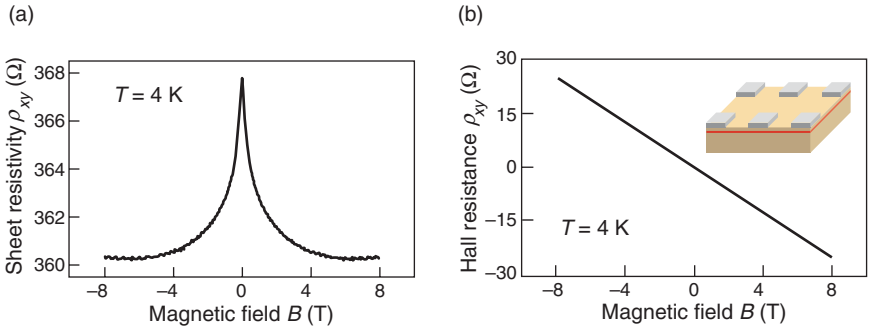

Figure 12. Electrical-Activity Tests
We wanted to check that phosphorus atoms incorporated in the silicon surface are electrically active. (a) The longitudinal resistivity ρ_{xx} of the delta-doped sample as a function of magnetic field was measured at 4 K. From this curve, a strong negative magnetoresistance is clearly observed, and it indicates the two-dimensional (2-D) nature of the delta-doped layer. (b) The Hall resistivity ρ_{xy} of the sample gives a 2-D carrier density of 2.0×10^{14} cm^{-2}. This number agrees with our dopant density and indicates that each phosphorus dopant is electrically active. The inset is a schematic of the phosphorus delta-doped silicon sample with metal surface contacts in the van der Pauw arrangement.

are incorporated in substitutional, rather than interstitial, sites, which is the ideal environment for the SSQC qubits.

Qubits, Defects, and Dopants

Although we have a clear strategy for creating and burying the phosphorus array, the volume surrounding the array in a working quantum computer must also be free from crystal impurities and defects. In general, defects disrupt the crystal structure and can create new pathways for quantum decoherence, which would inhibit qubit operations. Charged defects can be particularly disruptive. If the charge arises from an unpaired electron, then by necessity, there is an "impurity" spin that can interact with a qubit and affect its quantum state. Furthermore, the Coulomb potential of a charged defect lying close to a qubit can interfere with gate operations because it can offset the voltage applied to the qubit-controlling gate electrode.

Fortunately, the STM allows us to check the status of the buried qubits and charged defects during the fabrication of the quantum computer. Scanning tunneling microscopy is routinely used in characterizing the charge of individual defects found on the cleaved surfaces of compound semiconductors (Zheng et al. 1994, Lengel et al. 1994, Ebert et al. 1996). The charge becomes visible because of the so-called charge-induced band bending, illustrated in Figure 13. The states made available by band bending attract charge carriers that screen, or shield, the charged defect. Because bending shifts electronic states into or out of the window defining the source of the tunneling current, it produces a measurable enhancement or depression around the defect in the STM images. The characteristic length scale of this screening effect is given by the Debye screening length, which depends on the semiconductor's intrinsic properties: its dopant type and concentration (Dingle 1955).

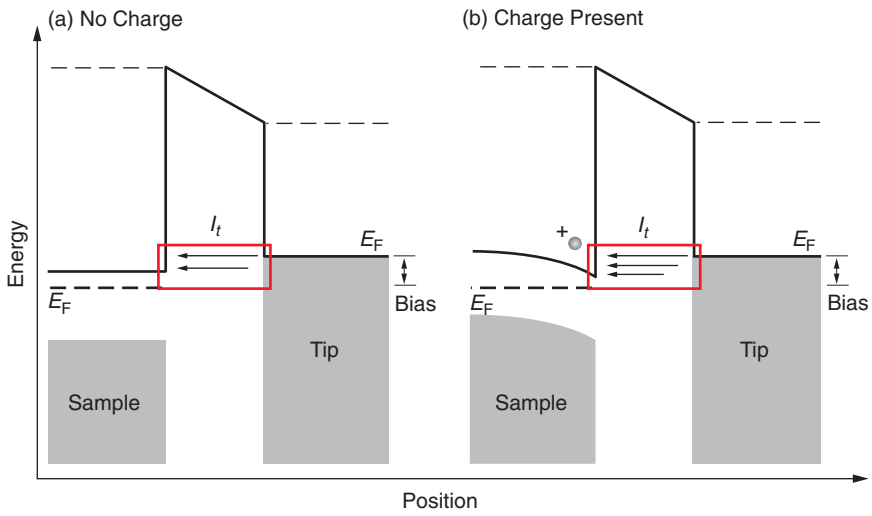

Figure 13. Band Bending
The electronic energy of an empty-state tunneling current is shown for a semiconducting sample with no charge (left) and with positive charge (right). The effects of surface states and defects have been neglected for illustration purposes. The charge-induced band bending shifts more states into the window between the Fermi levels of the tip and the sample. In this case, the increased state density relative to the rest of the neutral surface creates a long-range enhancement centered on the charge that falls off approximately like a screened Coulomb potential with a length scale set by the Debye screening length.

Table I. Expected Effect of Local Charge on Surface LDOS

Silicon(100)-2 × 1 Surface	Imaging Condition	+Charge	–Charge
***n*-type**	Empty states	Enhanced	Depressed
	Filled states	No effect	Enhanced
***p*-type**	Empty states	Enhanced	No effect
	Filled states	Depressed	Enhanced

These techniques for imaging charge have not been demonstrated on silicon surfaces until now because it has been generally assumed (based on techniques such as photoelectron spectroscopy that probe large surface areas) that the Fermi level at the surface of silicon is pinned. If that assumption is true, the bands cannot respond to charge near the surface. But by taking into account what occurs locally and by drawing on other results obtained with the STM, we have determined that pinning of the Fermi level does not occur for clean Si(100)-(2 × 1) surfaces, except in the vicinity of type-C defects. This has allowed us to image charged defects on these clean surfaces for the first time (Brown et al. 2002).

Considering the band structure as it is currently understood, we can qualitatively determine which types of charge should be detectable in filled- and empty-state imaging on a clean

silicon(100)-(2 × 1) surface for both *p*-and *n*-type materials.[3] These predictions, made under the assumptions of nondegenerate doping, a tip work function of 3 to 4 electron volts, and a low C-defect density, are compiled in Table I. As noted in the table, under some conditions, we anticipate no change in the appearance of an STM image. That result is singularly different from what is seen on compound semiconductors and arises from surface states derived from the π-bond. These states, which are not present on the compound semiconductor surfaces, limit the amount of band bending that can occur.

Based on the expectations listed in Table I, we performed STM experiments at sample biases between ±1.5 volts on clean (2 × 1) surfaces of Si(100) samples doped with phosphorus (approximately 8×10^{15} phosphorus atoms per cubic centimeter). Low sample biases were used to ensure that effects near the band edges (for example, band bending) contributed strongly to the tunneling current. In these experiments, we were able to image charged defects consistent with our *n*-type predictions.

One such charged defect is shown in Figure 14. This defect is commonly observed in studies of Si(100)-(2 × 1) surfaces on thermally prepared samples and is typically referred to as a split-off dimer (SD, also called the 1+2 DV) defect. It consists of an A- and a B-defect on the same row, separated by one intact dimer. The empty-state image of the SD defect shows a long-range perturbation, but the filled-state image shows no corresponding feature even though the filled-state imaging is closer to the valence band edge on this *n*-type material.

These results are consistent with expectations based on Table I, indicating positive charge associated with the SD defect. The enhanced density of states—bright region in Figure 14(b)—appears to be nearly radially symmetric and approximately centered on the defect structure. Sections through the data show that the signature is discernible out to about 4.5 nanometers from the center. The corresponding Debye screening length, obtained from a screened Coulomb potential function fit to the sections, is approximately 3 nanometers. That result was unexpected. The typical bulk value for the screening length that is consistent with our dopant density (which correlates with the number of charge carriers) is several tens of nanometers. The short screening length indicates a high dopant density at the surface. One explanation is that, on our thermally prepared surface, buried dopants may diffuse because of the high

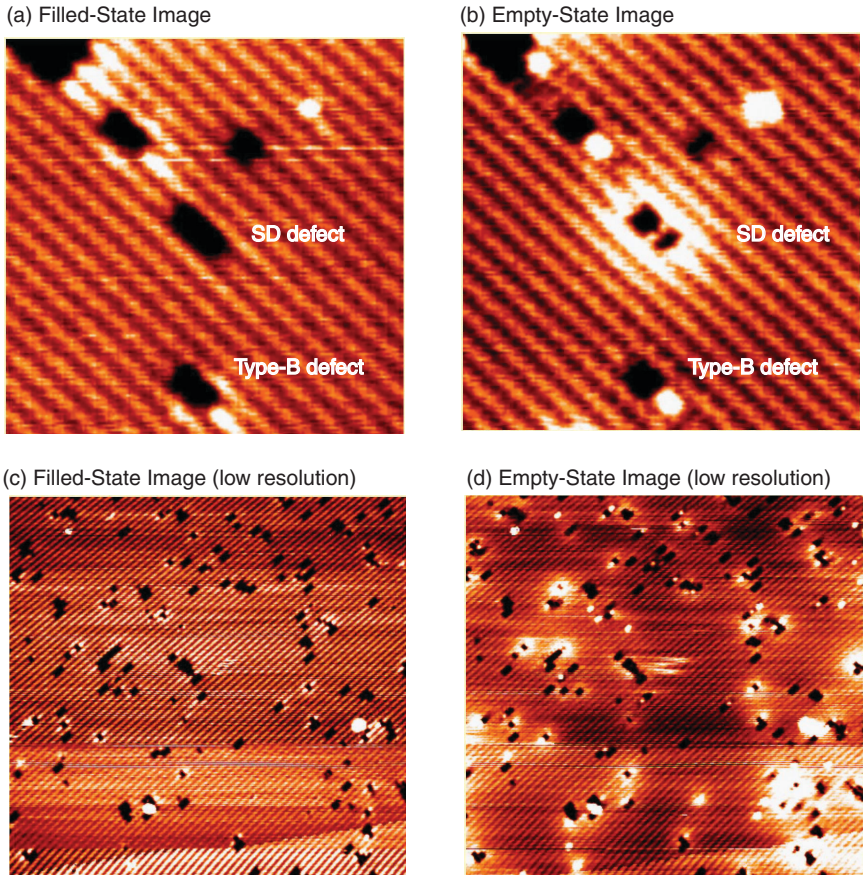

Figure 14. Finding Charged Defects

(a) This filled-state image shows a charged split-off dimer (SD) defect on a Si(100)-(2 × 1) surface (center) and a type B defect (bottom center). (b) The same defects are shown for an empty-state image. The bright "cloud" in the empty states around the central defect indicates that there is an associated positive charge. The other defects in the image appear neutral. These images measure 16.8 nm × 16.8 nm and were acquired "simultaneously" by raster scans interleaved at each bias. The asymmetric nature of the screening signature in the two biases is consistent with our expectations. (c)–(d) Pictured here are filled- and empty-state images from a different sample, taken at lower resolution. Only about one-third of the defects are charged. The images are 57 nm × 55 nm.

[3] Electrical conduction in *n*-type materials is associated with electrons. In *p*-type materials, it is associated with holes.

temperature, and the actual density at the surface could be high enough to account for the 3-nanometer screening length.

Another interesting result is that, for samples with defect densities less than 5 percent, only about one-third of the surface defects are charged. This finding tells us that the charge is not associated with the simple vacancy structure observed in the images but must arise from more subtle effects. Charged defects may be due to, for example, rebonding differences among second-layer atoms. Charged and neutral defects may also coexist because of subsurface impurities or gas-phase species adsorbed in the vacancy structure itself. At this point and by using only scanning tunneling microscopy, we are unable to ascertain why only some defects are charged.

The fact that charge can be imaged on a silicon surface tells us that, after creating a flat overlayer, we will be able to detect the subsurface charged qubits. This finding is important for determining whether the qubits move during subsequent silicon growth. And looking beyond the Kane architecture, our results will be applicable to any implementation of a solid-state, silicon-based quantum computer.

Future Challenges

To date, we have demonstrated most of the individual steps required to successfully fabricate the Kane SSQC. We can create a small phosphorus array (O'Brien et al. 2001) and incorporate that array into the silicon surface. We have shown that the phosphorus atoms remain electrically active (oberbeck et al. 2002). We can grow silicon epitaxially in the STM at a temperature that should leave the array intact, and we can detect charged defects at the surface. Although not reported in this article, the Semiconductor Nanofabrication Facility housed at the University of New South Wales in Sydney, Australia, has fabricated metallic gates with dimensions close to those required for proper operation of the quantum computer.

As we integrate the aforementioned steps and try to produce a few-qubit device, several questions remain to be answered. Will the qubit array stay intact during silicon overgrowth and during any required postanneals? Can we remove defects during fabrication and, if not, to what extent will vacancies or impurities affect the computer operation? Will we introduce charge defects at the interface between the silicon overlayer and the insulating layer? How well can we register the gates with the qubits, once the array has been built?

Still, the number of questions that confront us today is far smaller than the number that faced us three years ago, when we first contemplated the steps involved in fabricating the SSQC. At that time, each question was tied to a long list of experimental obstacles that needed to be overcome. Through the combined efforts of two laboratories in the United States and Australia, we have been able to develop experimental procedures that have moved us closer to fabricating a qubit array. Given our prior success, we are hopeful that the remaining issues can be addressed successfully as well.

On a different note, one exciting idea that has emerged recently is the possibility that STM can detect single spins. Yshay Manassen et al. (2000) reported detection of a spin-induced alternating-current component in the STM tunneling current. Recent theoretical work, discussed in the article "Theory of Single-Spin Detection with a Scanning Tunneling Microscope" on page 184, offers an explanation and puts the experimental finding on firmer ground. At Los Alamos, we are in the process of modifying the electronics of our STM and adding an external magnetic field with the hope of confirming the effect. If we are successful, directly studying spin-spin interactions and creating, manipulating, and reading out surface-bound qubits may become reality. Such a possibility is indeed exciting. ■

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Marilyn E. Hawley received her Ph.D. in physics from The Johns Hopkins University in 1987. Marilyn joined Los Alamos National Laboratory as a postdoctoral fellow in 1989. She was the first to successfully image and identify the spiral growth mechanism in high-temperature superconducting films using scanning tunneling microscopy (STM), results that were featured on one of the covers of Science. Marilyn has over 18 years of experience in STM and many advanced atomic force microscopy techniques. In 1991, she became a staff member in the Center for Materials Science at Los Alamos. Later, Marilyn established the Scanning Probe Microscopy Laboratory, a facility devoted to the development and use of scanning probe techniques for research on a broad spectrum of materials. She currently leads the Los Alamos STM team in an effort aimed at fabricating a qubit array for a possible future solid-state quantum computer.

Geoff Brown received a bachelor's degree in physics from Abilene Christian University and a Ph.D. in physics from Texas A&M University, where he studied the physics and chemistry of semiconductor surfaces using scanning tunneling microscopy (STM). In 1996, Geoff started at Los Alamos as a postdoctoral fellow in the Center for Materials Science, and he is now a technical staff member in the Scanning Probe Microscopy Laboratory at Los Alamos. His research involves STM and atomic-force microscopy studies of a wide range of materials, including semiconductors, complex oxides, metals, and superconductors.

Michelle Y. Simmons is currently the Director of the Atomic Fabrication Facility and a Queen Elizabeth II Research Fellow at the University of New South Wales, in Sydney, Australia. She joined the Centre for Quantum Computer Technology as the Program Manager in Atomic Fabrication and Crystal Growth in 2000, after completing a postdoctoral fellowship at the University of Cambridge, in the United Kingdom, where she was in charge of the design, fabrication, and characterization of ultrahigh-quality quantum electronic devices. She has over 14 years of experience in all aspects of semiconductor crystal growth, device fabrication, and electrical characterization of quantum electronic devices. Her current research interests are to understand how quantum electronic devices work as they become purer and smaller and to use this knowledge toward building the next generation of devices by using quantum principles—in particular a silicon-based quantum computer.

For the biography of Robert Clark, see page 300.

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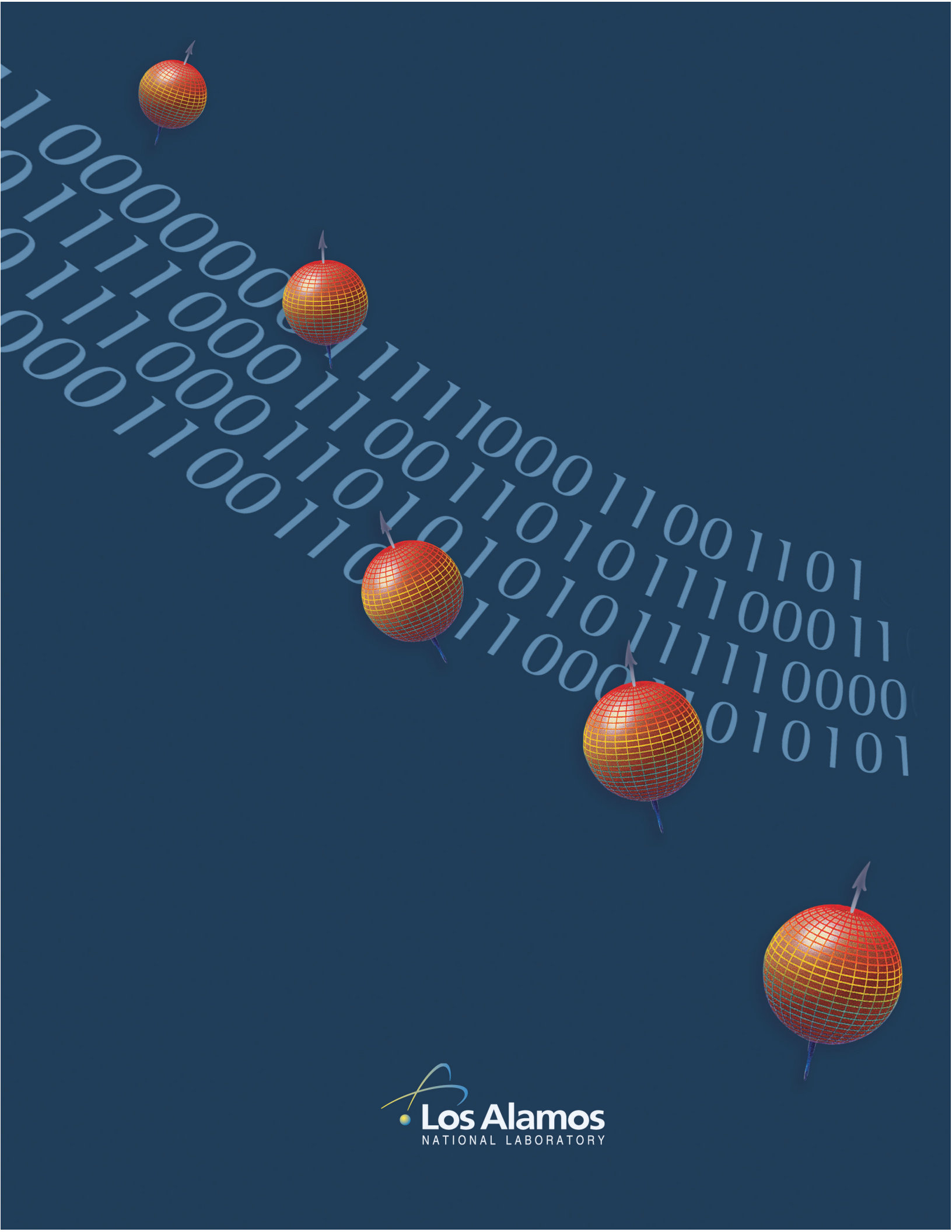
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